FSBB200-GaN — GaN ZVS Four-Switch Buck-Boost

FSBB200-GaN-xxT

Non-Isolated, Regulated DC-DC Converter

Features & Benefits

- Four-switch buck-boost (FSBB) topology
- Full ZVS on all four GaN switches
- Up to 200 W output power
- Input bus range: 21 – 37 V_{DC}
- Regulated output voltage (set by DCX ratio)
- Full GaN design using EPC eGaN® FETs
- Up to 98 % peak efficiency
- 507 W/in^3 power density
- Primary current sensing feedback
  - No direct output voltage sensing required
  - Ultra-wide regulation bandwidth
  - Fast transient response
- Integrated UVP, OVP, OCP & OTP protections
- $\overline{EN}$ enable pin (active low), autonomous start-up
- Non-isolated — pre-regulator for LLC DCX

Typical Applications

- Pre-regulator for LLC DCX bus converter
- 48 V intermediate bus architecture (IBA)
- Satellite & space power conditioning
- Telecom power distribution
- Industrial wide-input power systems
- Battery-fed voltage stabilization

Product Ratings

V_{IN} = 21 – 37 V	P_{OUT} = 200 W
V_{OUT} = 12 – 40 V (adj.)	I_{OUT} up to 8 A

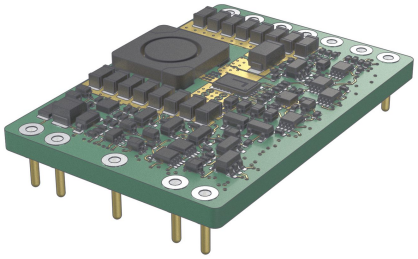
Product Description

The FSBB200-GaN is a non-isolated, regulated four-switch buck-boost DC-DC converter designed as a pre-regulator stage ahead of an LLC DCX bus converter. By regulating the intermediate bus voltage, the FSBB enables the downstream LLC to operate at its optimal fixed-frequency resonant point (DCX mode).

A key innovation is the use of primary-side current sensing of the LLC transformer as the feedback signal, eliminating direct output voltage measurement. This provides significantly wider control bandwidth and faster transient response. All four GaN switches achieve ZVS across the full operating range.

Package Information

- Through-hole pin module package
  - 45 × 31 × 10.08 mm [1.772 × 1.221 × 0.397 in]
  - Weight: 45 g [1.59 oz]
- 12 through-hole pins on two rows
- Operating temp: −40 to +105 °C



Typical Application

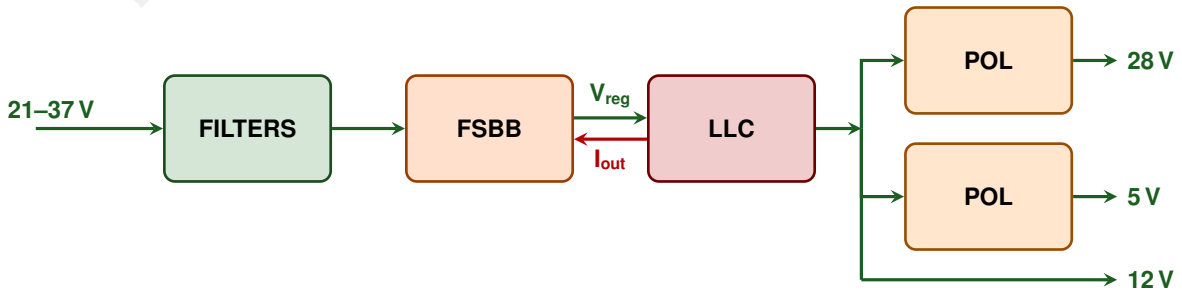


Figure 1 — System architecture: input filter + FSBB200-GaN pre-regulator + LLC DCX transformer + downstream POL regulators

Pin Configuration

Pin	Signal Name	Type	Function
1, 2	V_{IN}	INPUT POWER	Positive input power terminals (internally paralleled)
3	$\overline{EN}$	INPUT	Enable, active low. High stops the converter; low or open, the converter starts autonomously after ≈1 s (starter charge)
4, 5	0V	INPUT RETURN	Power return, input side (common ground)
6, 7	0V	OUTPUT RETURN	Power return, output side (common ground, non-isolated)
8	I_{BUF}	INPUT	Buffered output-current information from the DCX (or other downstream converter). Compensates the resistive voltage drop and regulates V_{BUS} without isolated voltage feedback
9	EN_{LLC}	OUTPUT	Connects to the corresponding LLC pin to disable the LLC input UVLO and operate in cascaded mode
10	V_{THRESH}	INPUT	Output (V_{BUS}) voltage setpoint adjustment — see the setting guide in the Recommended Land Pattern page
11, 12	V_{BUS}	OUTPUT POWER	Regulated output bus terminals (internally paralleled)

Pin numbering per the recommended land pattern (page 5): pins 1–5 on the input row, left to right; pins 6–12 on the output row, right to left (counter-clockwise numbering), module viewed from the top side.

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device. Electrical specifications do not apply when operating beyond rated operating conditions.

Parameter	Comments	Min	Max	Unit
Input Voltage (+IN to IN RTN)		−0.5	45	V
Output Voltage (+OUT to OUT RTN)		−0.5	45	V
Output Power			200	W
Operating Temperature Range	T-Grade	−40	+105	℃
Storage Temperature		−55	+125	℃
Lead Temperature (soldering)	10 s max		300	℃
Average Output Current			8	A

Part Ordering Information

Part Number	V_{OUT} range	Temperature Grade
FSBB200-GaN-T	12 – 40 V (adjustable)	T = −40 to +105 ℃

Note: Output voltage is continuously adjustable from 12 V to 40 V via the V_{THRESH} pin. The final load voltage is determined by the combination of V_{BUS} and the downstream DCX turns ratio: $V_{LOAD} = V_{BUS} / N$.

Safety and Reliability

Parameter	Comments	Min	Typ	Max	Unit
Insulation	Non-isolated topology		N/A		
MTBF	MIL-HDBK-217F, 25 ℃		2.0		MHrs

Electrical Specifications

Specifications apply over the full input range, T_{CASE} = 25 °C, V_{OUT} = 36 V unless otherwise noted. ***Boldface*** *specifications apply over the full temperature range.*

Attribute	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specifications					
Input Voltage Range	Continuous operation	**21**	28	**37**	V
Inrush Current (Peak)	Full resistive load			12.0	A
Input Current (no load)	$\overline{EN}$ low (enabled)		25	50	mA
Input Current (disabled)	$\overline{EN}$ high		2	5	mA
Power Output Specifications					
Output Voltage	Regulated, via V_{THRESH}	**12**	36	**40**	V
Output Voltage Accuracy	@V_{OUT} = 36 V, full load, 25 °C	−1.0		+1.0	%
Rated Output Power	Continuous			**200**	W
Rated Output Current	@V_{OUT} = 36 V			**5.6**	A
Maximum Output Current	Short duration			8.0	A
Output Current Limit	Of rated I_{OUT} max	110	130	150	%
Efficiency (@V_{OUT} = 36 V)					
Eff. @100 % load, 28V_{IN}		96.5	**97.5**		%
Eff. @50 % load, 28V_{IN}		97.0	**98.0**		%
Eff. @100 % load, 21V_{IN}	Boost mode	95.5	97.0		%
Eff. @100 % load, 37V_{IN}	Buck mode	96.0	97.5		%
Peak efficiency	Over full operating range		**98.0**		%
Regulation Performance					
Line Regulation	21 – 37 V		±0.1	±0.3	%
Load Regulation	10 – 100 % load		±0.2	±0.5	%
Output Ripple	BW 20 MHz, 100 % load		40	100	mV_{pp}
Transient Response	25–75 % load step, ΔV			2.0	%
Recovery Time	25–75 % load step		50	100	µs
Control Bandwidth	Primary current sensing		80		kHz
Dynamic Specifications					
Switching Frequency		450	500	550	kHz
Turn-on Delay	From $\overline{EN}$ falling edge	0.5		5	ms
Turn-off Delay	From $\overline{EN}$ rising edge			500	µs
Autonomous Start Delay	$\overline{EN}$ open, starter charge		1		s
Soft Start Ramp Time	Full rated resistive load		5	15	ms
Control Pins					
$\overline{EN}$ ON Threshold	Logic low			1.2	V
$\overline{EN}$ OFF Threshold	Logic high	3.3			V
V_{THRESH} Pin Range	Sets V_{BUS} setpoint	0.5		2.5	V
EN_{LLC} Output	Cascaded mode, UVLO disable		3.3		V
Protections (UVP / OVP / OCP / OTP)					
Input UVP Threshold		18		20	V
Input UVP Recovery			21		V
Input OVP Threshold				40	V
Input OVP Recovery			37		V
Output OVP Threshold	Latched shutdown		42		V
Output OCP Threshold	Of rated I_{OUT}	130		150	%
OCP Response Time				10	µs
Overtemperature (OTP)	Internal			115	°C

Mechanical Specifications

Parameter	Value	Unit
Overall Dimensions (L × W × H, pins included)	45.00 × 31.00 × 10.08	mm
	1.772 × 1.221 × 0.397	in
PCB thickness	2.54	mm
Tallest component above board	2.34	mm
Pin protrusion below board	5.20	mm
Mass	45	g
Mounting	Through-hole pins	—
Pin count	12	—
Pin material	Gold over nickel	—

Package Drawings

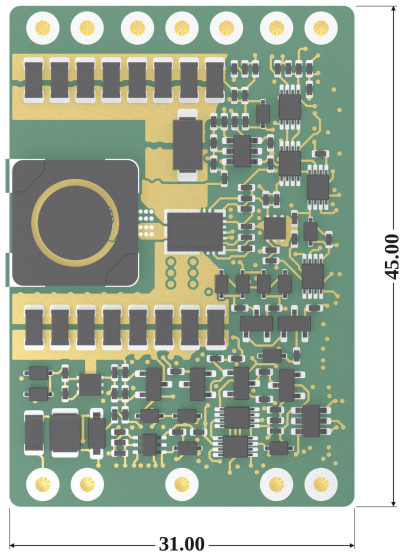


Figure 2 — Top view

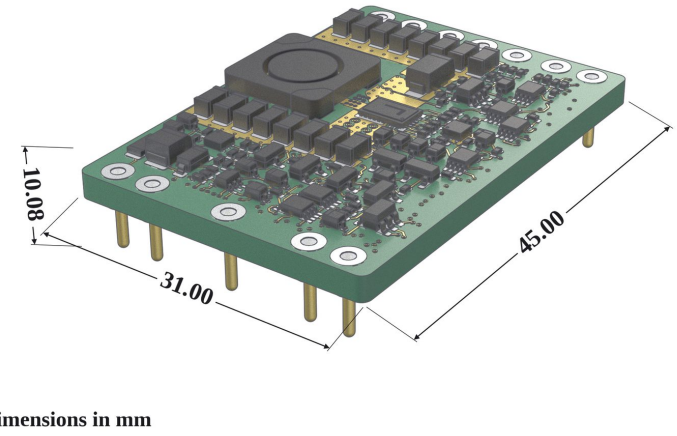


Figure 3 — Isometric view

Figure 4 — Side view

All dimensions in mm. Dimensions measured on the 3D CAD model (STEP).

Recommended Land Pattern

Recommended PCB land pattern, viewed from the **top (component) side**. The module mounts with 12 through-hole pins on two rows spaced 41.0 mm apart: input/control row (pins 1–5) and output row (pins 6–12). Pin 1 (V_{IN}) is identified by the corner index mark. Pin numbering is counter-clockwise, consistent with the DCX100-GaN. All dimensions in mm; geometry per mechanical drawing V2.

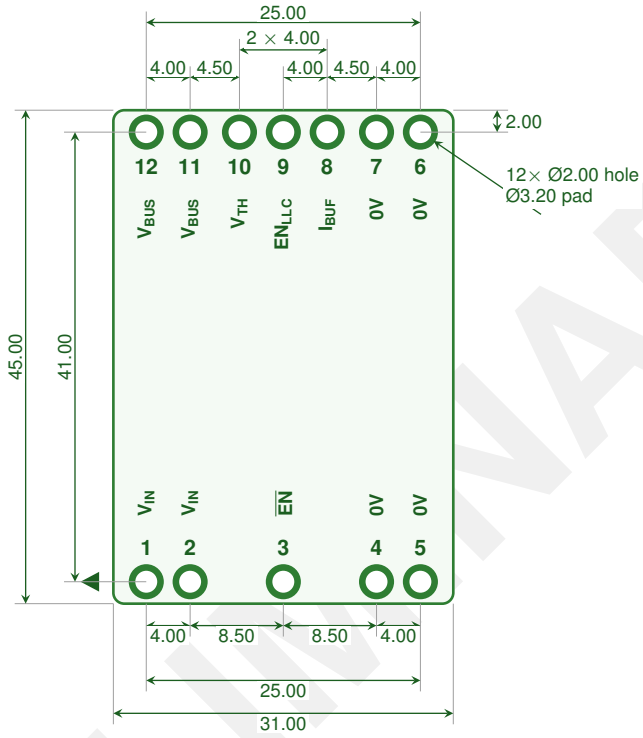


Figure 5 — Recommended land pattern (top view, component side). Corner radius 1.0 mm.

Parameter	Value	Note
Hole diameter	2.00 mm	12 positions, plated through-hole
Recommended pad diameter	3.20 mm	Annular ring ≥0.6 mm
Row spacing (pad centers)	41.00 mm	Input/control row to output row
Pad row to board edge of module	2.00 mm	Both rows

Application note — Setting the output voltage with V_{THRESH}

The V_{THRESH} pin sets the regulated bus voltage V_{BUS} of the FSBB200-GaN. In a cascaded FSBB + DCX architecture, the setpoint should be chosen so that (i) the downstream DCX operates near the middle of its input range, and (ii) sufficient headroom remains for the resistive-drop compensation performed through I_{BUF}. Detailed setting values (resistor divider on V_{THRESH} vs. target V_{BUS}, and their interaction with the I_{BUF} droop-compensation gain) are under characterization and will be published in the next revision of this datasheet. Contact POWCOMA for preliminary configuration support.