ADHA Power Module: Architecture and Measured Performance of the Engineering Model

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***Abstract*—This paper presents the power module of the Advanced Data Handling Architecture (ADHA), an ESA initiative standardizing on-board data handling units around the CompactPCI Serial Space backplane. The module integrates a nominal and a redundant $203\,\mathrm{W}$ power chain in a single 6U board. Each chain cascades two soft-switched GaN cells: a four-switch buck-boost (FSBB) pre-regulator under quadrangle control at $292\,\mathrm{kHz}$, and an LLC cell operated as a DC transformer (DCX) at its resonant frequency. The FSBB timings minimizing the inductor RMS current are computed offline over the full operating plane and approximated by analog circuits; no digital controller is used. Switching timings measured on the engineering model over 223 operating points are confronted with the recomputed optima: the analog implementation carries a median RMS excess of 16–$19\,\%$ above half load. Measured efficiency at ambient reaches $90.8\,\%$ with all outputs loaded and $92.1\,\%$ without the $28\,\mathrm{V}$ rail; the estimated loss breakdown identifies the litz LLC transformer as the dominant contributor. A second part details the evolutions prepared for the qualification model (QM): a revised architecture (point-of-load $5\,\mathrm{V}$, single-point $12\,\mathrm{V}$ regulation, integrated output protections, improved FSBB control) and planar magnetics. The predicted gain is one efficiency point at the worst-case operating corner and two points on average over the operating range.**

***Index Terms*—ADHA, power module, DC-DC converter, four-switch buck-boost, LLC, DCX, GaN, soft switching, quadrangle control, space power electronics.**

I. Introduction

On-board data handling equipment is traditionally mission-specific, with recurring qualification effort and little reuse. The Advanced Data Handling Architecture (ADHA) defines instead a standardized ecosystem of interoperable and interchangeable modules on a common CompactPCI Serial Space frame [1]. Within an ADHA unit, the power module conditions the $28\,\mathrm{V}$ unregulated platform bus into the secondary rails used by all other modules. It embeds a nominal and a redundant chain in one 6U equipment and, since it may supply vital loads, contains no permanently latching protection.

The converter differs from classical space power supplies on three points. (i) The complete chain is soft-switched: a four-switch buck-boost (FSBB) pre-regulator under quadrangle control [2]–[4] achieves zero-voltage switching (ZVS) on all four transistors, and the isolation stage is an LLC cell operated as a DC transformer (DCX) [6], [7]. This enables GaN devices [8] at frequencies that shrink magnetics and filters. (ii) The FSBB timing set minimizing the inductor RMS current [2], [5] is computed offline over the whole $(V_{\mathrm{in}}, P_{\mathrm{out}})$ plane and approximated by analog circuits: most of the benefit of an optimized modulation is obtained without a space-qualified digital controller. (iii) The engineering model (EM) characterized here implements conventional wound magnetics on RM cores; possible evolutions toward planar, PCB-integrated components [13], [14] are presented for the next model.

The paper is organized in two parts. Sections II–V document the EM as built and tested: architecture, FSBB control optimization and its measured distance to the optimum (223 operating points), DCX cell, efficiency maps and losses. Section VI presents the evolutions prepared for the qualification model (QM)—revised architecture and planar magnetics—and their predicted gains.

II. Main Requirements

Table I summarizes the main requirements applicable to the power chain and to the module.

TABLE I: Main Power Module Requirements

Parameter		Min	Max
Input voltage	(28 V nominal)	21 V	37 V
+5 V output	voltage	4.4 V	5.4 V
	current	0 A	5 A
+12 V output	voltage	10.6 V	12.6 V
	current	0 A	12.5 A
+28 V output	voltage	25.6 V	29.3 V
	current	0 A	1 A
Output power			203 W
Efficiency	($P_{\mathrm{out}} > 30\,\%$)	90 %	
Module mass			2.25 kg
Dimensions			$220 \times 233 \times 25\,\mathrm{mm}$

Each power chain is supplied through a single R-LCL or SO-LCL and starts up autonomously when the input voltage is in range. Current telemetry is provided on the $+5\,\mathrm{V}$ and $+12\,\mathrm{V}$ outputs.

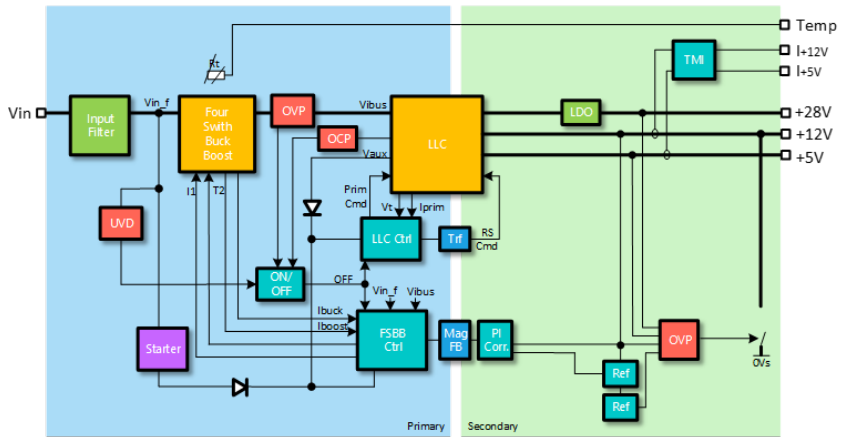


Fig. 1: Power chain block diagram of the EM. The FSBB regulates the intermediate bus $V_{\mathrm{bus}} = 35\,\mathrm{V}$; the DCX stage provides isolation and the secondary rails. The regulation loop is closed through the isolated feedback (PWM, capacitive isolation, filtering); all control functions are analog.

III. Power Chain Architecture

This section describes the chain as implemented on the EM; the evolutions prepared for the QM are gathered in Section VI.

A. Block Diagram

Each chain follows Fig. 1: an FSBB pre-regulator followed by an isolated DCX stage.

- *Input filter*: ECSS-compatible [9], integrating differential- and common-mode stages;
- *FSBB cell*: regulates $V_{\mathrm{bus}} = 35\,\mathrm{V}$ from an input above or below it, at fixed 292 kHz, with ZVS on the four switches (Section III-B);
- *DCX cell*: LLC stage locked on its series resonant frequency (200 kHz), providing isolation and a fixed gain [6], [7]. On this version, synchronous rectifiers are used on both the 12 V and the 5 V outputs; a 30 V winding feeds the 28 V LDO (Section III-D);
- *Isolated feedback*: the regulation error is converted into a PWM signal, transmitted through a triplicated capacitive isolation barrier, then filtered back on the primary side to drive the FSBB command;
- 28 V *LDO*: the rail supplies pulsed telecommand loads at low duty ratio; a linear post-regulator gives tight regulation and low output impedance with negligible average dissipation;
- *Protections*: primary undervoltage detection (UVD), OVP and OCP on the intermediate bus, and output overvoltage protection by crowbar of the 12 V rail with converter stop, whose measured response is reported in Section IV (Fig. 10). On this version the 5 V and 28 V rail protections are not integrated; they are in the QM architecture (Section VI);
- *Starter*: autonomous start-up sequencing from the primary bus.

All switches are EPC GaN transistors. Both switching frequencies are bounded by the response time of the analog driving chain (comparator, logic, GaN driver).

B. FSBB Cell: RMS-Optimal Quadrangle Control

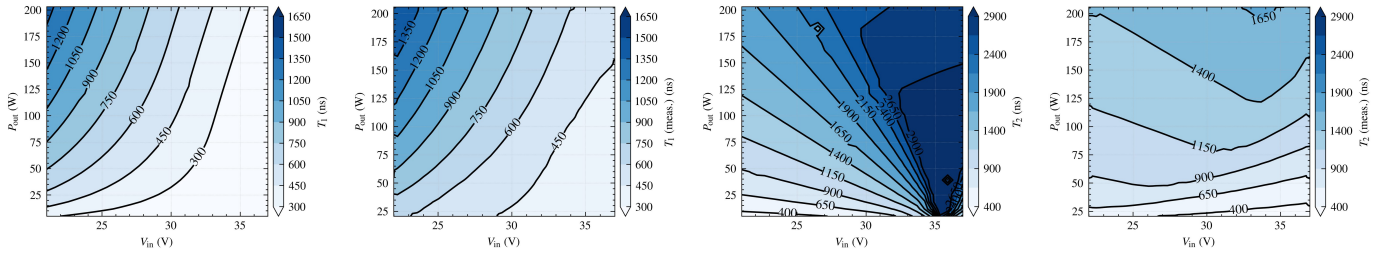
Under quadrangle control [2] the period splits into four intervals: magnetization (T_1, $v_L = V_{\mathrm{in}}$), direct transfer (T_2, $v_L = V_{\mathrm{in}} - V_{\mathrm{bus}}$), demagnetization ($T_3$, $v_L = -V_{\mathrm{bus}}$) and freewheeling (T_4). The current valley $-I_{\mathrm{zvs}}$ provides ZVS on the four switches; on the EM it is fixed at 1.6 A (dead time ≈ 35 ns). Table II lists the cell parameters.

TABLE II: FSBB Cell Parameters on the EM

Parameter	Symbol	Value
Input voltage range	V_{in}	21–37 V
Intermediate bus	V_{bus}	35 V (regulated)
Output power	P_{out}	0–203 W
Switching frequency	F_s	292 kHz (fixed)
Inductance	L_{BB}	1.4 μH
ZVS valley current	I_{zvs}	1.6 A (fixed)
Dead time	T_d	≈ 35 ns

With T_3 fixed by volt-second balance and T_4 by the fixed period, the command reduces to (T_1, T_2). For each $(V_{\mathrm{in}}, P_{\mathrm{out}})$ the timing set minimizing I_{rms} is computed offline by a deterministic solver (feasible-set seeding, SLSQP polishing of the exact piecewise-linear RMS expression [2]). Figs. 2(a) and (c) show the resulting optimal durations T_1 and T_2: these two maps fully define the FSBB command over the operating plane. Reproducing them exactly would require a digital controller. Instead, simplified functions extracted from the maps, driven by the regulation error, are implemented with analog circuits; Section III-C quantifies what this approximation costs.

Fig. 3 shows the corresponding optimal I_{rms} map: the RMS current is essentially set by the input current, and therefore grows towards low line and high load. The worst case is at $V_{\mathrm{in}} = 21\,\mathrm{V}$, 203 W: $I_{\mathrm{rms}} = 10.8\,\mathrm{A}$, $I_{\mathrm{pk}} = 19.5\,\mathrm{A}$ ($T_1 = 1406$ ns, $T_2 = 1825$ ns).



(a) T_1, optimal (b) T_1, measured (c) T_2, optimal (d) T_2, measured

Fig. 2: FSBB control durations: offline RMS-optimal maps (a), (c) and maps measured on the EM over 223 points (b), (d). Color scales and levels are identical between optimal and measured maps.

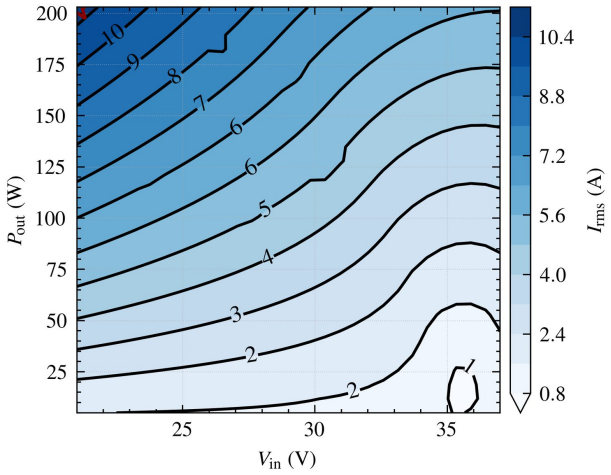


Fig. 3: Optimal inductor RMS current ($V_{\mathrm{bus}} = 35\,\mathrm{V}$, $F_s = 292\,\mathrm{kHz}$, $L_{\mathrm{BB}} = 1.4\,\mu\mathrm{H}$, $I_{\mathrm{zvs}} = 1.6\,\mathrm{A}$). The star marks the worst case.

C. Measured Waveforms and Distance to the Optimum

Fig. 4 shows the measured cell waveforms at low line: the trapezoidal inductor current with its negative ZVS valley, and zero-voltage commutation of both half-bridge nodes.

(a) no load (b) full load

Fig. 4: Measured FSBB waveforms at $V_{\mathrm{in}} = 21\,\mathrm{V}$: input half-bridge voltage (blue), output half-bridge voltage (red), inductor current (orange).

The timings T_1–T_4 were extracted automatically (high-resolution oscilloscope, Rogowski probe) over 223 operating points covering 22–37 V and loads up to full power (203 W). Figs. 2(b) and (d) map the measured T_1 and T_2 on the same scales as the optima. The measured maps reproduce the overall shape of the optimal ones—T_1 growing towards low line and high load, T_2 towards high line—but the analog law visibly departs from the optimum at light load, where it maintains longer powering intervals, and compresses the T_2 range at high line.

For each measured point, the cell waveform reconstructed from the timings gives the RMS current actually imposed by the analog control (Fig. 5). The optimum delivering the same output current under identical conditions (V_{in}, effective bus voltage from volt-second closure, measured frequency, 1.6 A valley, $L = 1.44\,\mu\mathrm{H}$ fitted) is then recomputed, and Fig. 6 maps the relative excess.

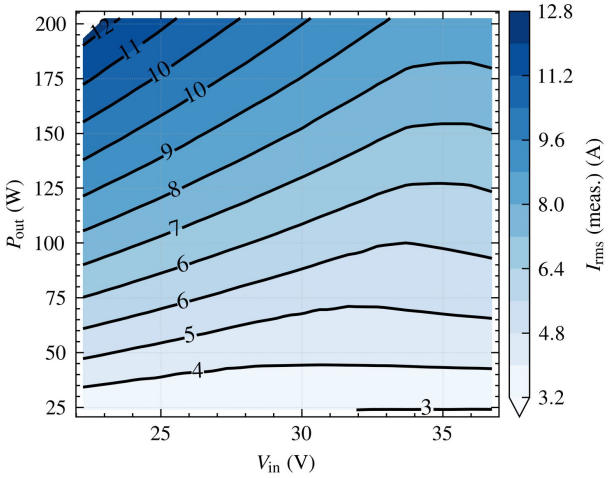


Fig. 5: Cell RMS current imposed by the analog control, reconstructed from the timings measured on the EM.

The median excess is 19 % over the full grid (6.8 vs. 5.6 A on average), 18 % between 100 and 150 W, 16 % above 150 W. It grows beyond 100 % at light load and high line, consistently with the deviations visible in Fig. 2(b). At the thermally dimensioning corner (low line, full load) the 16 % RMS excess translates into roughly one third more conduction loss than the theoretical minimum—the price of a fully analog, IC-free control. On the QM, the analog shaping functions are refined against these measured maps, targeting the recovery of most of this excess (Section VI).

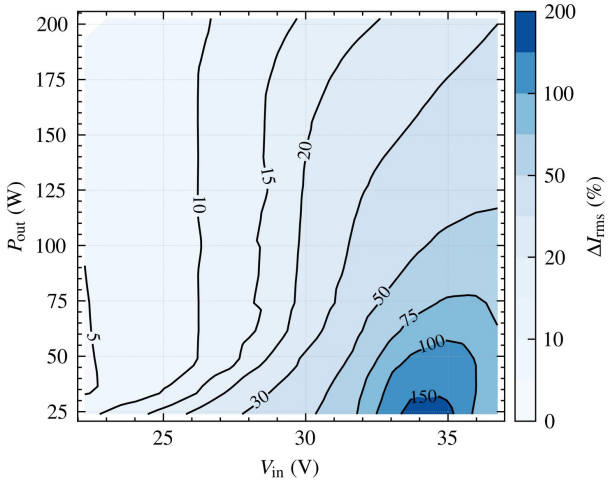


Fig. 6: Relative RMS-current excess of the implemented control with respect to the optimum.

D. DCX Cell

The LLC cell is self-oscillating and locked on the series resonance: unity gain, quasi-sinusoidal tank current, soft switching of primary switches and synchronous rectifiers [6], [7]. Operated as a DCX, it needs no control loop; only the primary current limitation and the start-up sequencing act on it.

On the EM the transformer carries three secondaries (5 V, 12 V center-tapped, 30 V for the LDO), wound in litz wire on an RM core. Cross-regulation between the 5 V and 12 V rails imposes a high turns count. Table III reports the measured impedances and the resulting loss estimate at the nominal operating point [13]: 8.7 W total, more than half in the primary winding. The secondary leakage inductances (100–700 nH) ring on the synchronous rectifiers and impose snubbers. Both observations drive the redesign of Section VI.

TABLE III: EM Litz Transformer: Measured Impedances and Loss Estimate

Quantity	Pri	12P	12M	5P	5M	28P	28M
R_{DC} (mΩ)	9.2	12	13	8	7.75	285	242
R_{AC} (mΩ)†	22	16	16.5	9	10	405	425
R_{AC}/R_{DC}	2.4	1.33	1.27	1.13	1.29	1.41	1.76
L_f (nH)	540	210	205	110	102	660	720
Loss (W)	4.56	1.54	1.63	0.15	0.16	0.24	0.22

†at 200 kHz. Core loss 0.20 W; total 8.71 W at nominal operating point.

IV. Engineering Model

The EM is shown in Fig. 7. The nominal and redundant chains are implemented vertically; GaN transistors and the most dissipative components are thermally connected to the cover housing (top cooling).

Fig. 8 shows a thermal image at full load, at an ambient temperature of 23 °C and without the mechanical frame (worst case for the top-cooled parts). Temperatures are absolute: the hottest switch reads 53 °C and the transformer 35 °C, i.e. rises of about 30 K and 12 K above ambient, leaving comfortable margins for operation in the frame.

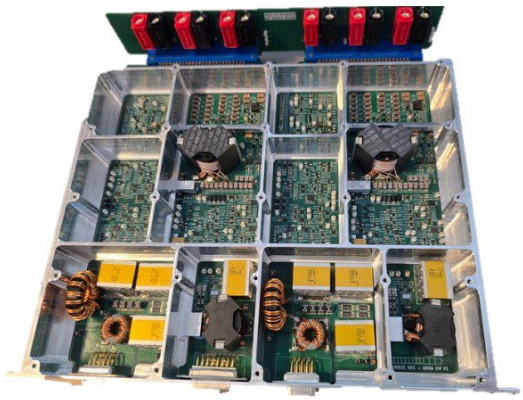


Fig. 7: ADHA power module engineering model.

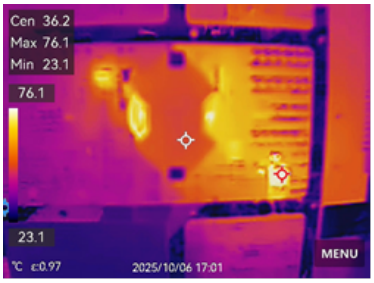


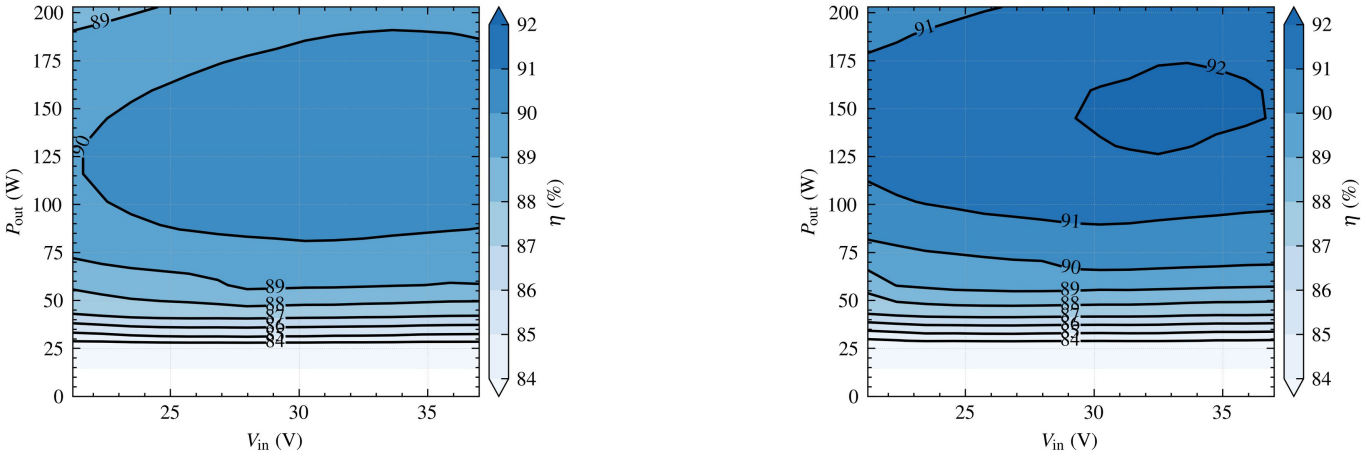
Fig. 8: Thermal image of the EM at full load, ambient, without mechanical frame.

The EM completed a full characterization and qualification campaign: start-up, protections (UVD, OVP), voltage accuracy, load transients, stability and output impedance. Stability margins (> 6 dB gain, $> 50°$ phase) and output impedance are compliant over the whole electrical and thermal range. Fig. 10 shows the measured response of the 12 V crowbar OVP: when the overvoltage threshold is crossed, the OVP signal trips, the synchronous-rectifier commands stop and the crowbar discharges the 12 V rail while the converter is stopped, without any permanent latching.

V. Measured Module Performance

The module efficiency was mapped at ambient over the full electrical range (automated bench, 15×15 grid, rails loaded proportionally). Fig. 9(a) shows the map with all outputs loaded, Fig. 9(b) without the 28 V output—representative of the mission profile, the telecommand rail being loaded only in short pulses. Both maps share identical color scales and levels for direct comparison.

With all outputs loaded the efficiency peaks at 90.8 % near 130 W and exceeds 89.5 % from 40 % load upwards;



(a) all outputs loaded

(b) 28 V output unloaded

Fig. 9: Measured EM efficiency at ambient temperature. Levels and color scales are identical on both maps.

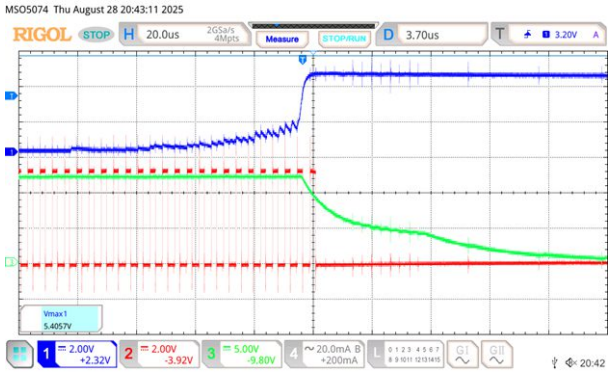


Fig. 10: Measured 12 V overvoltage protection: OVP signal (blue), 12 V output (green), synchronous-rectifier commands (red). 20 μs/div.

at full load it spans 88.6 % (low line) to 89.6 % (high line). Without the 28 V rail the map shifts up by about 1.5 points (peak 92.1 %, 90.5–91.3 % at full load): the difference directly measures the dissipation of the LDO architecture chosen for the telecommand rail. The low-line drop follows the FSBB RMS map (Fig. 3); the light-load roll-off combines the fixed losses of the two cells with the control excess of Fig. 6.

At the worst-case corner ($V_{in} = 21$ V, full load) the losses concentrate in two contributors: the litz DCX transformer (8.7 W, Table III), which alone exceeds the complete FSBB cell dissipation, and the FSBB conduction losses carrying the 16 % RMS excess of Section III-C. The estimated breakdown is compared with the QM prediction in Section VI-C (Fig. 14). These two mechanisms bound what the QM can recover.

VI. Evolutions Toward the Qualification Model

The second part of this work addresses the efficiency limitations identified above and upgrades the system performance. It combines a revised architecture and two planar magnetic components (the single multi-output DCX transformer and the FSBB inductor); the conversion principles of Fig. 1 are unchanged.

A. Revised Architecture

Fig. 11 shows the QM architecture. Three evolutions:

- the 5 V rail is generated by a qualified point-of-load converter [12] supplied from the 12 V output. Synchronous rectification remains only on the 12 V; the transformer loses two windings and the cross-regulation constraint on the turns ratio disappears;
- the 5 V and 28 V output protections, external on the EM, are integrated;
- the FSBB analog shaping functions are refined against the measured maps of Fig. 2, targeting the recovery of most of the 16 % worst-case RMS excess quantified in Section III-C.

Beyond efficiency, this architecture strongly improves the regulation performance. On the EM, the isolated feedback regulates a weighted combination of the 5 V and 12 V rails (barycentric regulation), so neither rail is individually tight. On the QM, the 12 V becomes the single regulated output, and the 5 V has its own dedicated POL loop: both rails gain static accuracy and dynamic response, and the load-transient coupling between rails disappears.

B. Planar Magnetics

DCX transformer. The single multi-output transformer, reduced on the QM to two secondaries (12 V / 30 V), migrates to a planar structure [10] whose layer arrangement is obtained by direct optimization of the magnetomotive-force distribution under the full leakage matrix [13]. Table IV summarizes the predicted gain against the measured litz baseline: the transformer loss falls from 8.7 to 4.2 W at the nominal point (Fig. 12), and the secondary leakage drops from 205 to 9.3 nH, allowing the removal of the secondary snubbers.

FSBB inductor. The inductor migrates to a PCB-integrated design with single-sided compensation of the air-gap fringing

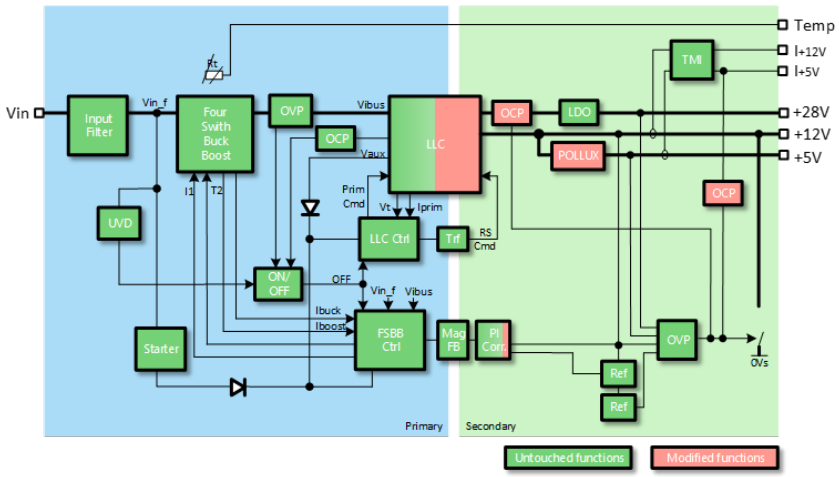


Fig. 11: QM power chain: 5 V POL supplied from the 12 V output, integrated output protections, single multi-output planar DCX transformer.

TABLE IV: DCX Transformer: Measured Litz Baseline vs. Predicted Planar Design (Nominal Operating Point)

Losses (W)	Litz (as built)	Litz (iso-arch.)†	Planar (3-D FE)
Primary	4.56	4.56	1.66
12 V P	1.54	1.54	0.71
12 V M	1.63	1.63	0.71
5 V (P+M)	0.31	–	–
30 V	0.46	0.46	0.10
Core	0.20	0.20	1.04
Total	**8.71**	**8.40**	**4.22**

†litz baseline with the 5 V windings removed, isolating the technology gain (50 %) from the architecture gain. Data from [13].

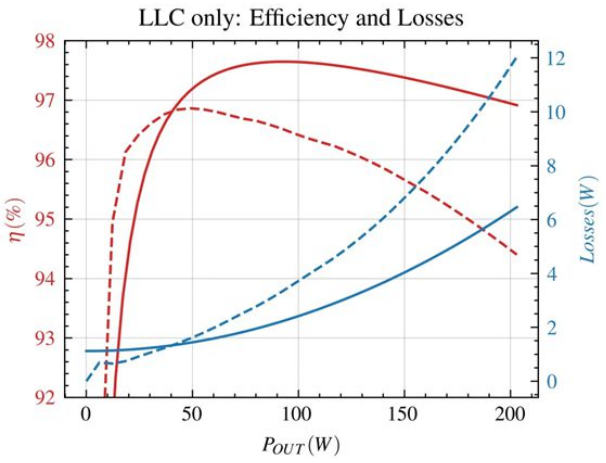


Fig. 12: DCX cell efficiency: optimized planar transformer (predicted) vs. EM litz configuration (measured).

field [11], sized by the RMS optimizer of Section III-B for operation at 450 kHz with 1.7 W of magnetic loss [14]. Fig. 13 shows the exploded view of the three-piece core and PCB winding; planar construction additionally brings the dimensional reproducibility that a wound RM component cannot guarantee in production.

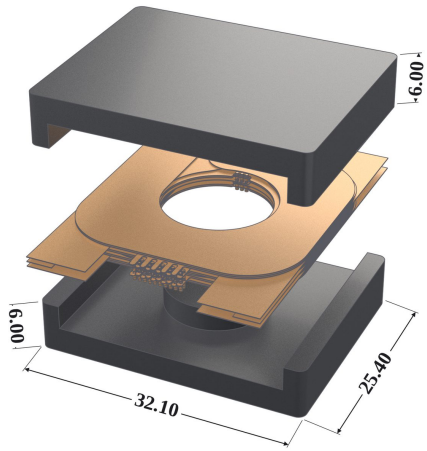
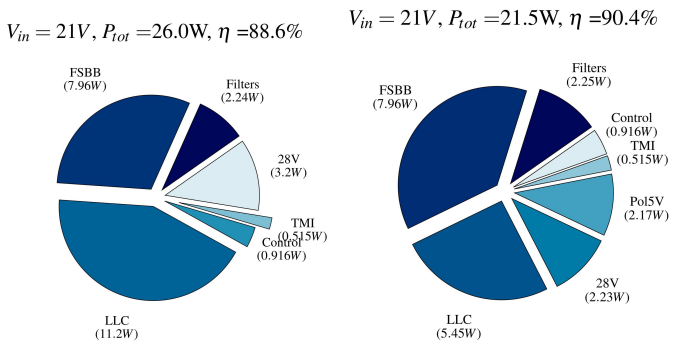


Fig. 13: PCB-integrated FSBB inductor: exploded view of the three-piece core and winding layers [14].

C. Predicted Performance

Fig. 14 compares the estimated loss breakdown of the EM at the worst-case corner ($V_{\text{in}} = 21$ V, full load) with the prediction for the QM configuration. The transformer share, dominant on the EM, is halved by the planar migration; the POL adds its own dissipation on the 5 V path, but the net balance remains clearly favourable. Combining the measured EM data with the planar transformer and POL models, the QM gains one efficiency point at the worst-case corner and two points on average over the operating range. The efficiency requirement of Table I is then met with margin over the whole plane, while the removal of the secondary snubbers

and the single-point regulation further improve robustness and regulation quality.



(a) EM (estimated) (b) QM (predicted)

Fig. 14: Loss breakdown at the worst-case operating corner ($V_{\mathrm{in}} = 21\,\mathrm{V}$, full load).

VII. Conclusion

A fully redundant, 203 W, three-rail power module has been implemented in a single 6U CompactPCI Serial Space board using two cascaded soft-switched GaN cells and purely analog control. The EM, built with wound RM magnetics, completed its full electrical characterization — start-up, protections, load transients, stability and output impedance — with comfortable thermal margins; measured efficiency at ambient reaches $90.8\,\%$ with all outputs loaded and $92.1\,\%$ without the $28\,\mathrm{V}$ rail — the configuration representative of the mission profile.

Beyond the demonstration itself, the offline RMS optimization of the quadrangle control provides a quantitative reference against which the hardware can be judged. Confronting timings measured over 223 operating points with the recomputed optimal trajectories isolates the cost of the analog approximation — a 16–19 % median RMS excess above half load — from the intrinsic cell losses, while the loss localization designates the litz multi-output transformer as the dominant contributor. Together, these two results turn the measured maps into a design agenda: they identify precisely where the next iteration should invest, and how much it can expect to recover.

The QM implements this agenda. It combines a revised architecture (5 V POL, single-point 12 V regulation, integrated output protections, refined FSBB control shaping) with a single multi-output planar transformer and a PCB-integrated FSBB inductor. The predicted gain is one efficiency point at the worst-case corner and two points on average over the operating range, together with markedly improved regulation performance, the removal of the secondary snubbers, and the dimensional reproducibility required for recurring production. These evolutions consolidate the module as a standard building block for the ADHA ecosystem.

Acknowledgment

This work was carried out within the ADHA (Advanced Data Handling Architecture) project and is supported by the European Space Agency under contract 4000142637/23/NL/CRS. The authors warmly thank Hadrien Carbonnier for his support and guidance throughout the project.

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