Design and Experimental Validation of a PCB Integrated Inductor for Space Oriented Four Switch Buck Boost Converters

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Abstract*—This paper presents the complete design flow of a PCB integrated inductor for a $200\,\mathrm{W}$ ($210\,\mathrm{W}$ maximum), 21–$37\,\mathrm{V}$ input four-switch buck-boost (FSBB) converter switching at $450\,\mathrm{kHz}$. A timing optimization minimizing the RMS cell current under a fixed-dead-time zero-voltage-switching constraint yields the worst-case four-phase inductor current, which is then the sole excitation of the magnetic design. The air gap is opened on one face only—a single-sided variant of the compensating fringing-field concept—and its optimal placement is fixed, in normalized coordinates, by a parametric 2-D finite-element (FE) map that keeps $R_{\mathrm{AC}}/R_{\mathrm{DC}}$ below 1.20 while remaining compatible with a three-piece self-locating core. An analytical sizing procedure, combining the Dowell model for copper losses and MagNet-Hub for core losses, then selects the design of minimum board footprint under a $2.0\,\mathrm{W}$ loss budget. The core height is not a design variable: it follows from the normalized gap placement itself, which sets the distance between the gap and the first copper layer. The result is a three-turn design wound as four parallel sets on a twelve-layer board, occupying $11.3\times11.3\times6.5\,\mathrm{mm}$ and weighing $2.9\,\mathrm{g}$ of ferrite—one quarter of the litz-wire component it replaces. A tolerance analysis shows the air gap dominates the inductance spread ($\pm17\,\%$ RSS under standard $\pm50\,\mu\mathrm{m}$ machining tolerances) and identifies a moderate switching-frequency adjustment as the system-level lever that absorbs it. A 3-D FE analysis of the part as drawn—assembly clearances included—yields $0.957\,\mu\mathrm{H}$ and an AC-to-DC winding-resistance ratio of 1.62 at $450\,\mathrm{kHz}$, below the value assumed in sizing; the recomposed FE loss budget, $1.92\,\mathrm{W}$ at the worst case, holds the $2\,\mathrm{W}$ target. A hardware prototype is manufactured and characterized under representative operating conditions.

***Index Terms*—PCB integrated inductor, four-switch buck-boost converter, space power electronics, finite-element optimization, high-frequency losses, ZVS timing optimization, fringing-field compensation.**

I. Introduction

Four-switch buck-boost converters are attractive for applications requiring a wide input-to-output voltage range with bidirectional capability, such as battery-powered actuator drives and the power-processing units (PPU) of satellite platforms [2], where a regulated bus must be held across a wide, slowly drifting battery voltage. Wide-bandgap devices are now qualified for such equipment [3], which makes the switching frequency assumed here realistic in a space context. The topology imposes a non-sinusoidal, four-phase current waveform on its inductor, which complicates both the RMS current prediction and the design of the magnetic component. Modulation strategies that explicitly shape this current to reduce its RMS value are an active topic [4].

Quadrangle control—in which the inductor current is shaped into a trapezoid with a negative freewheeling plateau—is the established way to obtain ZVS on all four switches [5]. Liu *et al.* show that the total converter loss increases monotonically with the duration of the powering stage and accordingly select its smallest feasible value. Here we minimize the inductor RMS current directly, under a fixed-dead-time ZVS constraint, since it is that quantity—together with the flux excursion—which drives the magnetic design; we reuse the exact closed-form RMS and average current expressions derived in [5].

Planar magnetics implemented in printed-circuit-board (PCB) copper layers offer high power density, tight dimensional tolerancing, and compatibility with surface-mount assembly. However, the fringing field around the air gap of a conventional PCB inductor penetrates the winding from the side, driving skin and proximity losses that can substantially increase the AC-to-DC resistance ratio [1]. Schäfer *et al.* introduced the *compensating fringing field concept* (CFFC), in which the air gap is relocated above or below the PCB so that its fringing field counteracts the proximity field within the winding [1]. Here we apply a single-sided variant of this concept—with the air gap on one face only—realized on a fully custom ferrite core split into three pieces, so that the stack locates itself and needs no external mechanical structure.

This choice of a custom component is deliberate. Commercial off-the-shelf power inductors are specified almost entirely in the DC domain—saturation current, thermal rating, DCR—while the frequency-resolved AC resistance is seldom published, and when it is, for sinusoidal rather than four-phase excitation: a catalogue part can be *selected* on its DCR but not *sized* on its dissipation. The mechanism behind that missing figure is the one a DC-oriented design has no incentive to address—the gap fringing field couples into the winding and raises $R_{\mathrm{AC}}/R_{\mathrm{DC}}$ well above unity, by a factor set by the gap position [6], [8]. Here the AC harmonics carry $27\,\%$ of the squared current, enough for that penalty to dominate the loss

budget—precisely the term the CFFC suppresses [1].

The paper makes four contributions:

- A systematic timing optimizer for the FSBB that minimizes the inductor RMS current subject to a fixed dead-time ZVS constraint, and identifies the worst-case operating point over the full operating range.
- A parametric 2-D FE map of the single-sided CFFC that fixes the optimal gap placement in normalized coordinates, decoupling it from the core sizing, together with the quantification of the penalty incurred by opening the gap on one face only.
- An analytical design-space exploration combining Dowell copper-loss modeling and MagNet-Hub core-loss prediction, with a loss-budget footprint-minimization selection method, completed by a tolerance propagation onto the inductance value.
- A 3-D FE loss-extraction method matched to the FSBB waveform— per-harmonic AC-resistance solves for the winding and a single field-sensitivity map for the core—used to verify the analytical sizing and to refine the AC-resistance model.

II. FSBB Converter and Worst-Case Current

The FSBB cell consists of four switches Q_1–Q_4 and the inductor L_{BB}; its specifications are summarized in Table I. Under quadrangle control [5] the period is divided into four intervals, each defined by the conducting pair, and the inductor current is piecewise-linear on each of them (Fig. 1):

- T_1, *powering* (Q_1, Q_3): the inductor sits between V_{in} and ground, $v_L = V_{\mathrm{in}}$ and the current ramps up at V_{in}/L. The input charges the inductor; nothing reaches the load.
- T_2, *direct power path* (Q_1, Q_4): input and output are joined through the inductor, $v_L = V_{\mathrm{in}} - V_{\mathrm{out}} < 0$ at this corner; power flows to the load while the current decays. This interval is what makes the topology efficient—energy transits instead of being stored and restored.
- T_3, *reset* (Q_2, Q_4): the inductor sits between ground and V_{out}, $v_L = -V_{\mathrm{out}}$; the current falls steeply, still feeding the output, and crosses zero.
- T_4, *freewheeling* (Q_2, Q_3): both ends grounded, $v_L = 0$, the current holding at the valley $-I_{\mathrm{zvs}}$ that discharges the output capacitance of Q_1; its duration reconciles $T_1{+}T_2{+}T_3$ with the fixed period.

Volt-second balance over the period imposes

$$V_{\mathrm{in}}\,T_1 + (V_{\mathrm{in}} - V_{\mathrm{out}})\,T_2 - V_{\mathrm{out}}\,T_3 = 0, \tag{1}$$

and ZVS at every transition requires a negative valley current

$$I_{\mathrm{zvs}} = \frac{2\,C_{\mathrm{oss}}\,V_{\max}}{T_d}, \tag{2}$$

i.e. 1.4 A for the selected GaN device at $T_d = 50\,\mathrm{ns}$, held constant over the whole operating map.

Eliminating T_3 through (1) leaves (T_1, T_2) as the only free variables. The boundary currents follow directly,

$$I_1 = I_4 = -I_{\mathrm{zvs}},\quad I_2 = I_1 + \frac{V_{\mathrm{in}}T_1}{L},\quad I_3 = I_2 + \frac{(V_{\mathrm{in}}-V_{\mathrm{out}})T_2}{L}, \tag{3}$$

TABLE I
FSBB Converter Specifications

Parameter	Symbol	Value
Input voltage range	V_{in}	21–37 V
Output voltage	V_{out}	35 V (regulated)
Output power	P_{out}	0–210 W
Switching frequency	F_s	450 kHz
Inductance	L_{BB}	1.0 μH
Dead time	T_d	50 ns (fixed)

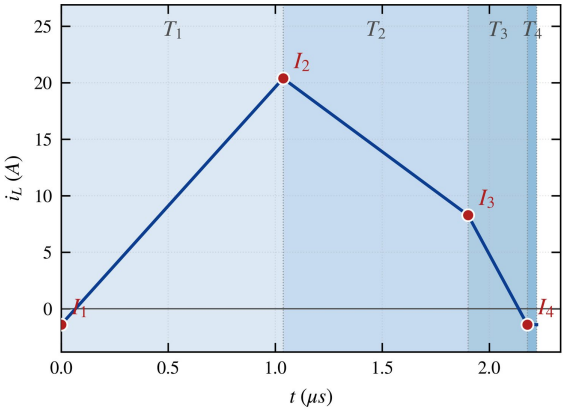

Fig. 1. Inductor current at the worst-case operating point ($V_{\mathrm{in}} = 21\,\mathrm{V}$, $P_{\mathrm{out}} = 210\,\mathrm{W}$, $F_s = 450\,\mathrm{kHz}$). Phase durations T_1–T_4 and current levels I_1–I_4 are indicated.

and the output current, delivered only while Q_4 conducts (phases T_2 and T_3), is

$$I_{\mathrm{out}} = \frac{1}{T_s}\left[\frac{I_2 + I_3}{2}T_2 + \frac{I_3 + I_4}{2}T_3\right]. \tag{4}$$

The RMS inductor current admits the closed form derived by Liu *et al.* [5, eqs. (5) and (10)],

$$I_{\mathrm{rms}}^2 = I_1^2 + \frac{I_1 V_{\mathrm{in}}(T_1{+}T_2)(T_1{+}T_3)}{L\,T_s} + \frac{V_{\mathrm{in}}^2(T_1{+}T_2)}{3\,T_s L^2}\left[T_1^2 + T_1T_3 + \frac{T_2T_3^2}{T_2+T_3}\right]. \tag{5}$$

Once (1) holds, (5) is *exact* for this waveform—no small-ripple approximation is involved—and we verified it against direct segment-by-segment integration of the piecewise-linear current to machine precision (1.5×10^{-16} relative at the worst-case point). A SLSQP optimizer minimizes I_{rms} in (T_1, T_2) subject to (1), (2), a freewheeling floor $T_4 \geq 0.02\,T_s$ and the power-transfer equality $I_{\mathrm{out}} = P_{\mathrm{out}}/V_{\mathrm{out}}$. The timing model is lossless, so that $V_{\mathrm{in}}\,\bar{\imath}_{\mathrm{in}} = V_{\mathrm{out}}\,I_{\mathrm{out}}$ holds exactly; this is the conservative choice for magnetic sizing, since a real conduction drop would be compensated by a marginally longer T_1 and hence a larger flux excursion.

Fig. 2 maps the resulting I_{rms} over the operating range. The maximum lies at minimum input voltage and maximum output power, $V_{\mathrm{in}} = 21\,\mathrm{V}$, $P_{\mathrm{out}} = 210\,\mathrm{W}$; Table II gives the corresponding timing and currents. At this corner the ZVS

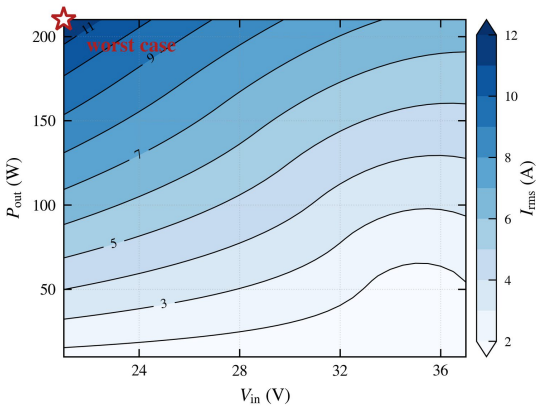

Fig. 2. Optimal inductor RMS current over the operating range ($V_{\text{out}} = 35\,\text{V}$, $F_s = 450\,\text{kHz}$, $L_{\text{BB}} = 1\,\mu\text{H}$). Each point minimizes I_{rms} under fixed-dead-time ZVS and exact power transfer.

TABLE II
OPTIMAL TIMING AND CURRENT AT WORST-CASE OPERATING POINT

Quantity	**Symbol**	**Value**
Phase 1 duration	T_1	1037 ns
Phase 2 duration	T_2	864 ns
Phase 3 duration	T_3	277 ns
Phase 4 duration	T_4	44 ns
ZVS valley current	$I_1 = I_4$	-1.40 A
Peak current	$I_{\text{pk}} = I_2$	20.38 A
Notch current	I_3	8.28 A
DC component	I_{dc}	10.39 A
RMS current	I_{rms}	12.14 A

constraint and the fixed frequency also bound the transferable power: 215.4 W at $L = 1.0\,\mu$H, 210 W at $1.03\,\mu$H—at 450 kHz the specified maximum power leaves almost no headroom on the inductance. This ceiling is a *timing* constraint, not a magnetic one—it scales with the switching period, reaching $1.16\,\mu$H at 400 kHz and $1.32\,\mu$H at 350 kHz—a degree of freedom the tolerance analysis of Section III-I returns to.

This waveform is the sole excitation of the magnetic design. Its harmonic content, obtained by FFT over one switching period, is given in Table III. The DC component alone carries 73 % of the squared current and the fundamental a further 26 %; the DC component and the first three harmonics together account for 99.88 % of I_{rms}^2, higher orders being negligible. The copper-loss summation in the remainder of this paper nevertheless retains all harmonics up to $n_h = 20$.

TABLE III
HARMONIC CONTENT OF THE WORST-CASE INDUCTOR CURRENT

	f (kHz)	$\hat{I}$ (A)	I_{rms} (A)	share of I_{rms}^2	cumul.
DC	0	10.39	10.39	73.23 %	73.23 %
h_1	450	8.70	6.15	25.68 %	98.91 %
h_2	900	1.07	0.76	0.39 %	99.30 %
h_3	1350	1.30	0.92	0.58 %	99.88 %
total			12.14	100 %	

III. PLANAR INDUCTOR DESIGN

A. Design Objectives and Scope

The compensating fringing-field concept (CFFC) of Schäfer *et al.* [1] is the starting point of this design. The contribution claimed here is not the concept but its reduction to an industrially usable form, along four axes:

- *Implementability*: a winding in standard PCB copper on a custom three-piece core that assembles without external hardware, with the performance quantified against the measured litz-wire component it replaces (Section III-B).
- *Single-sided air gap*: the two-sided arrangement of [1] needs a machined core half on each face; opening the gap on one face only has a cost, on the total loss and on the current distribution between layers, and that cost is quantified.
- *Manufacturing tolerances*, propagated onto the inductance value, since they govern reproducibility in volume.
- *Unit cost and series feasibility*.

Thermal validation is outside the scope of this paper and will be presented orally at the conference.

B. Baseline: the Previous Litz-Wire Inductor

The component this design replaces is a discrete inductor built on a commercial RM8 core set in 3C95 ferrite, wound with litz wire on a bobbin, characterized on an impedance analyser from 1 kHz to 8 MHz over ten repeated sweeps (reproducibility better than 0.1 % on L_s above 10 kHz). Table IV sets it against the design proposed here.

Two observations drive the redesign. First, the DC resistance dominates the loss budget: at 14.6 mΩ it dissipates 1.58 W on the DC component alone ($I_{\text{dc}} = 10.39$ A, Table II), because litz wire buys a favourable AC-to-DC ratio at the cost of the copper fill factor in the winding window [1]. Second, the measured terminal resistance ratio already reaches 1.98 at 450 kHz: the component is being pushed past the band its material is intended for, 3C95 being specified for power conversion up to 500 kHz whereas N49 is optimized for 300 kHz–1 MHz. Raising the switching frequency—which shrinks the filters and the inductance itself, from 1.53 to $1.0\,\mu$H—therefore requires a material change and a winding whose AC behaviour is designed rather than inherited.

C. Inductor Geometry and Parameterization

The inductor uses a custom EF-type ferrite core with a round centre leg and a PCB winding of N turns. The core is split into three pieces—an ungapped bottom half, a centre-leg spacer that sets the gap, and a top half—which locate on one another so that the stack is self-supporting and requires no external clamping structure (Fig. 8). Once the specification (L, I_{pk}, B_{sat}, $h_{\max}$, e_{Cu}, N) is fixed, the geometry is fully described by two independent variables (Fig. 3):

- r_C: radius of the centre leg;

TABLE IV
PREVIOUS LITZ-WIRE INDUCTOR VS. PROPOSED PLANAR DESIGN

Quantity	**Previous (litz)**	**Proposed (planar)**
Core	RM8 set (COTS)	custom, 3 pieces
Ferrite	3C95 ($\mu_i = 3000$)	N49 ($\mu_i = 1500$)
Material band	$\leq 500\,\mathrm{kHz}$	0.3–1 MHz
A_e (mm^2)	52	29.2
l_e (mm)	35.5	12.0
Winding	litz on bobbin	12-layer PCB
Integration	discrete, on board	winding in the board
L (μH)	1.527*	0.957‡
R_{DC} (mΩ)	14.62*	2.41‡
R_s at 450 kHz (mΩ)	28.94*	12.8‡
$R_{\mathrm{AC}}/R_{\mathrm{DC}}$ at 450 kHz	1.98*†	5.31‡

*Measured, mean of ten sweeps. †Terminal ratio: it includes the core-loss contribution seen in series and is therefore an upper bound on the winding-only ratio. ‡3-D FE on the final geometry, winding only, twelve-layer stack at the terminals, copper at 20 °C. Note that the proposed design shows the *higher* resistance ratio while carrying less than half the absolute AC resistance: the ratio is inflated by a DC resistance six times lower, and it is R_s, not $R_{\mathrm{AC}}/R_{\mathrm{DC}}$, that sets the dissipation. A like-for-like measured comparison, same instrument and same method, will be reported in Section V.

- r_B: radial width of the winding window.

All remaining dimensions follow. The yoke thickness x_C is set so that the yoke cross-section equals the centre-leg cross-section. The window height is not free either: the 2-D study of Section III-E fixes the optimal axial distance between the gap and the first copper layer at $0.4\,r_B$, so the window height is *constructed* as

$$z_C = 0.4\,r_B + t_{\mathrm{PCB}} + t_{\mathrm{m}}, \tag{6}$$

with $t_{\mathrm{PCB}} = 2.1\,\mathrm{mm}$ the twelve-layer board thickness and $t_{\mathrm{m}} = 0.5\,\mathrm{mm}$ the clearance under the board; the total height is therefore a derived quantity, not a design variable, and the optimal gap placement is preserved by construction at every point of the design space. The two flat yokes are manufactured thicker than the magnetic minimum x_C for robustness (1.6/1.2 against $0.8\,\mathrm{mm}$); the extra ferrite runs at proportionally lower flux density, a second-order loss contribution. The centre-leg cross-section and mean magnetic path length are $S_C = \pi r_C^2$ and $l_C = 2z_C + \frac{1}{2}r_C + 2r_B + \frac{1}{2}x_C$.

a) Air-gap length: Because the gap is a substantial fraction of the centre-leg diameter, its reluctance cannot be taken as $e_F/(\mu_0 S_C)$: the flux bulges radially and the effective gap area is larger than S_C. The gap required to reach the target inductance is therefore obtained from an uncorrected value e_{F0} scaled by a fringing factor F_f:

$$e_{F0} = \frac{\mu_0 N^2 S_C}{L}, \quad F_f = 1 + \frac{e_{F0}}{\sqrt{S_C}}\ln\frac{2\,l_C}{e_{F0}}, \quad e_F = F_f\,e_{F0}. \tag{7}$$

For the selected design $F_f = 1.26$, i.e. the physical gap is 26 % larger than the uncorrected value—an error far too large to neglect. The core reluctance term $l_C/\mu_r = 12\,\mu\mathrm{m}$ represents only 2.8 % of e_F and is neglected in (7).

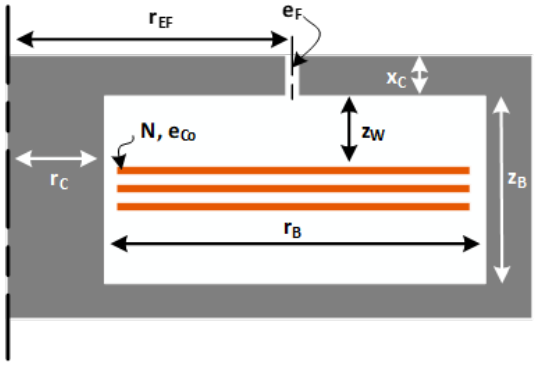

Fig. 3. Cross-sectional parameterization of the EF-core planar inductor. The air gap e_F is opened on the top face only (single-sided CFFC). The design variables are r_C and r_B; x_C, z_C and z_B are derived quantities.

b) Saturation constraint: The peak flux density must not exceed B_{sat}:

$$B_{\max} = \frac{L\,I_{\mathrm{pk}}}{N\,S_C} \leq B_{\mathrm{sat}}. \tag{8}$$

D. Compensating Fringing-Field Concept

In a conventional planar inductor the air gap lies in the centre leg, in the plane of the PCB winding. The flux bulging out of the gap crosses the copper tracks perpendicularly, induces eddy currents and reduces the effective conducting cross-section: the inner edge of the winding carries a strongly elevated current density and $R_{\mathrm{AC}}/R_{\mathrm{DC}}$ rises accordingly. This is the dominant AC loss mechanism in gapped planar magnetics, ahead of the inter-layer proximity effect; closed-form descriptions are given in [6] and, for gapped foil windings, in [7].

Two families of remedies exist. The quasi-distributed gap [8] splits the single gap into several weaker ones, at the cost of a machined or stacked centre leg. The CFFC of [1] takes the opposite route: the gap is displaced *away* from the winding plane, onto the face of the board, at a radius chosen so that its fringing field opposes the field the winding itself produces in the copper—a virtual anti-parallel current sheet cancelling the net transverse field over most of the winding width. The gap position thus becomes a genuine design variable with an optimum, which the 2-D study of Section III-E determines.

In [1] the gap is opened symmetrically on both faces, which doubles the compensation but requires a custom core half above *and* below the PCB. We restrict ourselves to a *single-sided* opening—gap machined on the top face only, ungapped bottom half, one shim. The compensation is then asymmetric, so its penalty is quantified rather than assumed small: in Section III-E for the loss, in Section IV for the layer-by-layer current distribution.

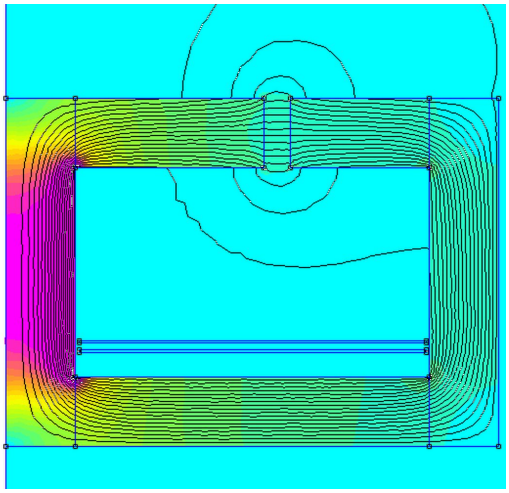

Fig. 4. Parameterized 2-D axisymmetric FE model (FEMM) of the single-sided CFFC inductor: flux lines and flux-density magnitude at peak current. The gap is opened on the upper face at radius r_{ef}; the winding layers appear as the thin rectangles in the window.

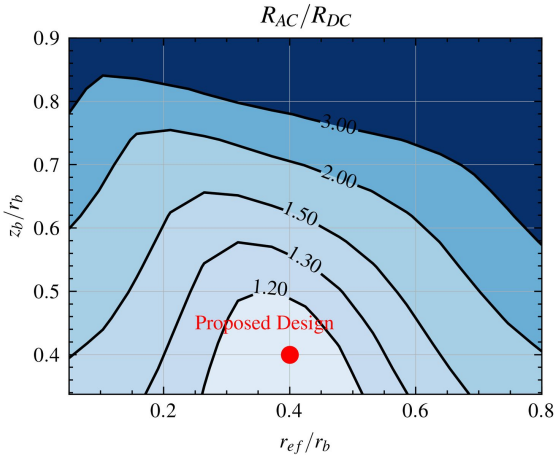

Fig. 5. $R_{\mathrm{AC}}/R_{\mathrm{DC}}$ of the PCB winding from the parametric 2-D FE sweep at $F_s = 450\,\mathrm{kHz}$, as a function of the normalized radial position r_{ef}/r_b and axial distance z_b/r_b of the single-sided gap. The selected design sits in the flat basin at $R_{\mathrm{AC}}/R_{\mathrm{DC}} < 1.20$.

E. Parametric 2-D FE Study and Optimal Gap Placement

The gap placement is optimized on a 2-D axisymmetric magnetoquasistatic model (Fig. 4) built in FEMM and driven by a script, so that the geometry is regenerated and re-meshed for every candidate. It contains the ferrite core, the winding resolved layer by layer and the single-sided gap; the mesh resolves the skin depth ($\delta_{\mathrm{Cu}} = 97\,\mu\mathrm{m}$ at $450\,\mathrm{kHz}$ and $60\,^{\circ}\mathrm{C}$) across the $70\,\mu\mathrm{m}$ track thickness, and returns the winding losses from which $R_{\mathrm{AC}}/R_{\mathrm{DC}}$ is extracted.

Two normalized parameters govern the compensation: the radial position of the gap r_{ef}/r_b and its axial distance to the winding z_b/r_b, both referred to the winding outer radius r_b. Sweeping the two yields the map of Fig. 5, the central design tool of this work. A well-defined optimum exists around $r_{\mathrm{ef}}/r_b \approx 0.4$ and $z_b/r_b \approx 0.4$, where $R_{\mathrm{AC}}/R_{\mathrm{DC}}$ stays below 1.20 against values above 3 for a badly placed gap. The map is markedly asymmetric: moving the gap axially away from the winding degrades the ratio much faster than moving it radially, so the PCB-to-core spacing—not the radial alignment—is the tolerance-critical dimension. The optimum is broad radially, any r_{ef}/r_b between 0.3 and 0.5 staying within 1.30, which is what makes the concept manufacturable with standard core tolerances.

The mechanism behind the map is resolved layer by layer by the 3-D FE extraction of Section IV (Fig. 9). Because the gap is opened on one face only, the compensation is inherently asymmetric: the layer facing the gap sees the fringing field directly and recovers a nearly uniform current distribution, while the layers beneath are increasingly screened and retain part of the proximity-driven crowding at the track edges. This residual asymmetry is the direct cost of the single-sided variant with respect to the two-sided arrangement of [1], and it motivates the layer-resolved AC-resistance model of Section III-F.

Fixing the gap placement in normalized coordinates decouples it from the core sizing: the design space of Section III-H is then explored in (r_C, r_B) alone, and the geometry carried over to the 3-D model of Section IV without re-optimizing the gap.

F. Copper Losses: Dowell Model

The AC resistance is computed with the Dowell model, applied harmonic by harmonic [9]. Dowell's one-dimensional assumption degrades for the wide, thin conductors of a planar winding; orthogonal field-decomposition models [10] bound the resulting error. For the k-th harmonic at frequency kF_s, the penetration ratio is

$$\xi_k = \frac{e_{\mathrm{Cu}}}{\delta_k}, \qquad \delta_k = \sqrt{\frac{\rho_{\mathrm{Cu}}}{\pi \mu_0 k F_s}}, \tag{9}$$

where ρ_{Cu} is corrected for temperature. Because the current carries a large DC component, the copper loss must retain the DC term explicitly; only the AC harmonics are subject to the resistance increase:

$$P_{\mathrm{Cu}} = \frac{R_{\mathrm{DC}}}{n_p} I_{\mathrm{dc}}^2 + F_{R,\mathrm{eff}}(N)\, R_{\mathrm{DC}} \sum_{k=1}^{n_h} I_{k,\mathrm{rms}}^2, \tag{10}$$

with $n_h = 20$ harmonics retained, R_{DC} the resistance of *one* set of N turns (11), and $n_p = 12/N$ the number of identical sets paralleled at the terminals of the twelve-layer board. The DC current divides evenly between the sets; the AC harmonics concentrate in the layers nearest the gap, so the AC term is conservatively kept at its single-set value (Section IV-D). The DC component alone carries $73\,\%$ of the squared current ($I_{\mathrm{dc}} = 10.39\,\mathrm{A}$ for $I_{\mathrm{rms}} = 12.14\,\mathrm{A}$); the parallel division is what keeps its loss below the AC term. The DC resistance follows from exact cylindrical integration of the spiral winding,

$$R_{\mathrm{DC}} = \frac{2\pi N\, \rho_{\mathrm{Cu}}}{e_{\mathrm{Cu}}\, \ln\!\big((r_C + t_i + r_B)/(r_C + t_i)\big)}, \tag{11}$$

t_i being the clearance between the centre leg and the innermost track. For the design-space sweep the per-harmonic Dowell factor is condensed into a single effective ratio applied to the AC harmonics,

$$F_{R,\mathrm{eff}}(N) = 1 + (F_{R,0} - 1)\, N^2, \tag{12}$$

where $F_{R,0} = 1.1$ is calibrated on the 2-D FE result of Fig. 5 at the optimum gap placement, and the N^2 law reflects the growth of the inter-layer proximity term with the number of layers [8], [9]. The layer-resolved picture of the 3-D FE extraction (Fig. 9) shows this ratio is not uniform—the layer facing the gap is nearly fully compensated while the layers beneath carry the residual proximity term—so (12) is an effective, winding-level quantity. An effective AC resistance $R_{\mathrm{AC}} = P_{\mathrm{Cu}}/I_{\mathrm{rms}}^2$, DC included, is reported throughout; it is *not* the same quantity as (12), being diluted by the DC term.

G. Core Losses: $B(t)$ and MagNet-Hub

Unlike resonant converters, whose quasi-sinusoidal current admits a single-frequency Steinmetz formula, the FSBB inductor carries the asymmetric four-phase waveform of Section II, and the core loss is *not additive over the current harmonics*: the loss of a sum of sinusoids differs from the sum of their individual losses, which is precisely why iGSE-type models [11] and the data-driven MagNet-Hub model [13] used here operate on the complete time-domain waveform. The large DC premagnetization—$I_{\mathrm{dc}} = 10.39\,\mathrm{A}$ for a peak of $20.38\,\mathrm{A}$—is a second reason: Steinmetz-derived formulations need explicit correction there [12], whereas networks trained on measured data cover it directly [14].

In the analytical model the flux density in the centre leg is derived from the reluctance model, assuming a spatially uniform flux density equal to the centre-leg value:

$$B(t) = \frac{L\, i_L(t)}{N\, S_C}. \tag{13}$$

Since $i_L(t)$ is piecewise linear, $B(t)$ is piecewise linear as well. The complete waveform—including the negative excursion during T_3—is evaluated once by MagNet-Hub to obtain the volumetric loss p_{Fe}, and the total is $P_{\mathrm{Fe}} = p_{\mathrm{Fe}} V_C$. The spatial non-uniformity of the flux, in particular the lower density in the yokes, is recovered by the 3-D method of Section IV.

H. Design Space and Selected Design

With the gap placement fixed in normalized form by Fig. 5 and the height constructed by (6), the design space reduces to (r_C, r_B) for each turn count. The scarce resource on a power module is board area, not height—the constructed height stays near $5\,\mathrm{mm}$ across the whole space—so the selection minimizes the *footprint*, i.e. the core side $2(r_C + r_B + x_C)$, subject to the total-loss budget $P_{\mathrm{tot}} \le 2.0\,\mathrm{W}$, about $1\,\%$ of the maximum output power. Fig. 6 shows the loss map for $N = 3$: the optimum sits where the smallest iso-footprint line still touches the region inside the $2\,\mathrm{W}$ contour, at $r_C = 3.05\,\mathrm{mm}$, $r_B = 1.72\,\mathrm{mm}$—a core of $11.3\,\mathrm{mm}$ side, with the budget exactly consumed. Section III-I describes how the three-piece mechanical realization departs slightly from this mathematical optimum, and why the departure is benign.

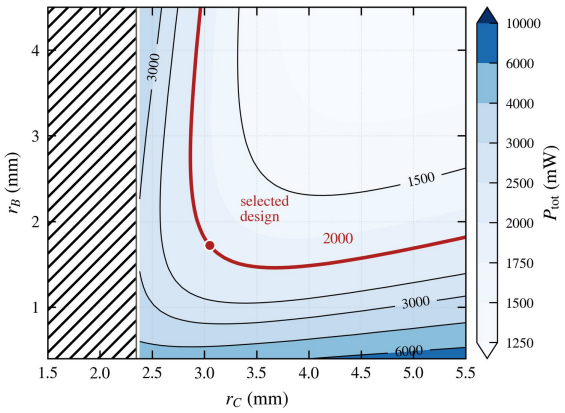

Fig. 6. Total-loss map over the design space (r_C, r_B) for $N = 3$ turns (four parallel sets) at the worst-case waveform, the core height being constructed by (6) at every point. The red curve is the $2\,\mathrm{W}$ budget; the marker is the footprint-minimal feasible point ($11.3\,\mathrm{mm}$ side); the hatched band is infeasible.

TABLE V
FOOTPRINT-MINIMAL POINT PER TURN COUNT UNDER THE 2 W BUDGET (TWELVE-LAYER WINDING, $12/N$ SETS IN PARALLEL)

Quantity	**Sym.**	N=1	N=2	N=3	N=4
Centre-leg radius (mm)	r_C	6.36	3.82	3.05	2.78
Window width (mm)	r_B	1.02	1.23	1.72	2.76
Height (mm)	h	7.73	5.66	5.07	5.02
Air-gap length (μm)	e_F	171	266	417	686
Peak flux (mT)	$B_{\max}$	160	222	232	210
Core volume (mm^3)	V_C	2803	801	511	504
R_{DC}/n_p (mΩ)		0.99	2.13	3.00	3.46
P_{Cu} (mW)		622	935	1223	1436
P_{Fe} (mW)		1377	1063	777	561
Core side (mm)		19.5	12.7	**11.3**	12.4

Table V repeats the exercise for $N = 1 \ldots 4$ ($12/N$ parallel sets). Every optimum consumes the budget exactly—the constraint is active—so the turn counts are discriminated by the footprint they need to dissipate $2\,\mathrm{W}$: as N increases the larger gap and lower flux density reduce the core loss, while the N^2 proximity penalty raises the copper loss, and the side is minimized at $N = 3$. Fig. 7 shows the corresponding split. The selected design is summarized in Table VI.

I. Manufacturing Tolerances

For a design whose performance rests on the placement of a gap relative to a winding, tolerance propagation is not a secondary concern. Differentiating the reluctance model (7) about the selected design gives the first-order sensitivities of the inductance:

$$\frac{1}{L}\frac{\partial L}{\partial e_F} = -0.166\,\%/\mu\mathrm{m}, \qquad \frac{1}{L}\frac{\partial L}{\partial r_C} = +0.063\,\%/\mu\mathrm{m}, \tag{14}$$

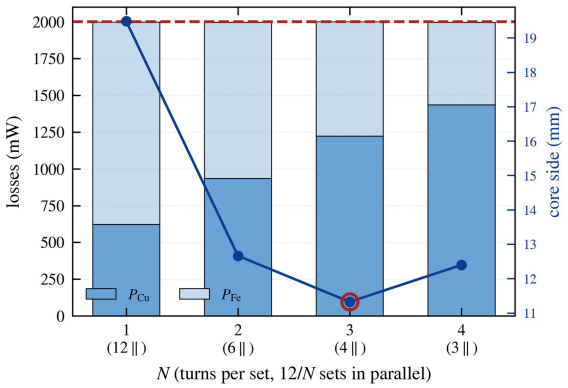

Fig. 7. Copper/core loss split and core side at the footprint-minimal point for each turn count N ($12/N$ parallel sets), the 2 W budget being exactly consumed in every case. Core loss falls and copper loss rises with N; the footprint is minimized at $N = 3$.

TABLE VI
SELECTED INDUCTOR DESIGN ($N = 3$, $P_{\text{tot}} \leq 2\,\text{W}$)

Parameter	Symbol	Value
Number of turns	N	3
Parallel sets	n_p	4 (12 layers)
Centre-leg radius*	r_C	2.80 mm
Window width	r_B	1.72 mm
Window height (6)	z_C	3.29 mm
Copper thickness	e_{Cu}	70 μm
Inter-layer clearance	t_i	100 μm
Air-gap length	e_F	500 μm
Fringing factor	F_f	1.26
Inductance, 3-D FE incl. clearances	L	0.957 μH
Peak flux density (at 0.957 μH)	$B_{\max}$	259 mT
Core volume, magnetic model	V_C	422 mm^3
Core volume, as drawn		619 mm^3 (2.9 g)
Total height, assembled	h	6.51 mm
Core footprint		11.3 × 11.3 mm
Core material		N49
DC resistance, one set	R_{DC}	11.23 mΩ
DC resistance, terminal	R_{DC}/n_p	2.81 mΩ
AC resistance, eff.	$P_{\text{Cu}}/I_{\text{rms}}^2$	7.52 mΩ
Copper losses	P_{Cu}	1026 mW
Core losses	P_{Fe}	636 mW
Total losses	P_{tot}	1662 mW

*Reduced from the 3.05 mm optimum to equalize the centre-leg and corner-post flux sections in the three-piece core; see the realized-core discussion in Section III-I.

while the sensitivities to the window width r_B and to the total stack height are three orders of magnitude smaller ($< 0.0005\,\%/\mu\text{m}$) and are negligible. This result is the useful one for production: the inductance is governed by the shim thickness and by the centre-leg diameter alone, and is essentially insensitive to the PCB stack-up and to the winding window.

The three ferrite pieces are machined to $\pm 50\,\mu$m, which is the tolerance class quoted by ferrite suppliers for ground faces on custom parts without an additional lapping operation. Since

TABLE VII
TOLERANCE BUDGET OF THE SELECTED DESIGN

Contributor	Tol.	Sensitivity	$\Delta L/L$
Air gap (two faces)	$\pm 100\,\mu$m	$-0.166\,\%/\mu$m	$\mp 16.6\,\%$
Centre-leg radius	$\pm 50\,\mu$m	$+0.063\,\%/\mu$m	$\pm 3.1\,\%$
PCB stack height	$\pm 50\,\mu$m	$< 0.001\,\%/\mu$m	negligible
Window width r_B	$\pm 50\,\mu$m	$< 0.001\,\%/\mu$m	negligible
Worst case			$\pm 19.8\,\%$
RSS			$\pm 16.9\,\%$

the air gap is bounded by two facing machined surfaces—the top half and the centre-leg spacer—the two tolerances add and the gap can depart from its nominal value by up to $100\,\mu$m, whereas the centre-leg diameter carries the single-part tolerance. Table VII propagates these figures.

The inductance therefore spreads over $\pm 20\,\%$ of the realized nominal in the worst case and $\pm 17\,\%$ in RSS, the air gap alone contributing $84\,\%$ of the budget. Because the sensitivity scales as $1/e_F$, the gap opened to $500\,\mu$m to absorb the assembly reluctances is not a concession but a gain: the same $\pm 100\,\mu$m machining band that would have cost $\pm 25\,\%$ at the ideal $348\,\mu$m gap costs $\pm 17\,\%$ here. Confronted with the timing ceiling of Section II—210 W deliverable only up to $L = 1.03\,\mu$H at 450 kHz—the residual spread still exceeds it: from $0.957\,\mu$H the RSS band tops out at $1.12\,\mu$H, above the 450 kHz ceiling but inside the $1.16\,\mu$H ceiling at 400 kHz. The resolution is thus *systemic* rather than magnetic: a moderate switching-frequency adjustment absorbs the complete manufacturing stack at no hardware cost [15]; the differential nature of the gap in the three-piece core (Fig. 8) is expected to tighten it further.

The gap is bounded by the top plate and the centre-leg stub, both machined to $\pm 50\,\mu$m; the four corner posts of the bottom piece locate the top plate laterally, so no external clamping or bonding fixture is required (Fig. 8).

The realized core departs from the mathematical optimum in two respects. First, equalizing the centre-leg section with the sum of the four corner-post sections—the posts being bounded by the board-egress windows—reduces the leg to $r_C = 2.80$ mm at unchanged footprint. Second, the assembly clearances—between the centre-leg stub, its seat and the top plate—add parasitic series reluctances that the ideal reluctance model (7) does not carry. The gap is therefore not transferred to the drawing at its nominal value: it is set on the 3-D FE model of the complete assembly, clearances included, which brings $e_F = 500\,\mu$m and $L = 0.957\,\mu$H, within $4\,\%$ of the $1.0\,\mu$H target. Reading the gap off the assembly rather than off the ideal model is what makes the two agree, and the larger gap that results is favourable on two counts: the flux excursion stays moderate ($B_{\max} = 259$ mT), and the relative sensitivity to the gap tolerance falls as $1/e_F$ (Section III-I). The air gap itself is a *differential* dimension—the height step between the corner posts and the centre leg, two faces of the

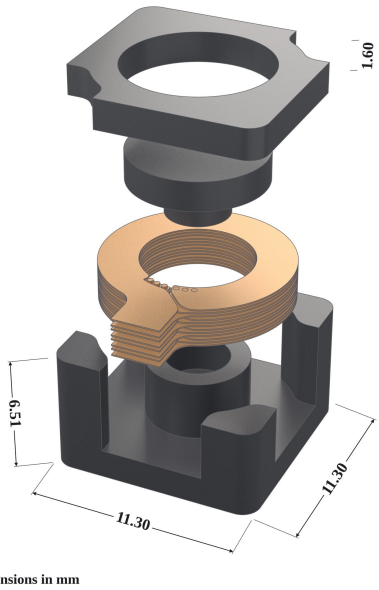

Fig. 8. Exploded view of the design, dimensions in mm: the gapped top plate carrying the centre-leg stub, the multi-layer PCB winding with its plated vias, and the bottom piece whose four corner posts receive the top plate. The stack locates on itself and needs no external clamping; the winding is a section of the motherboard, so the core adds no height beyond its own.

same machined part—so its tolerance should hold well below the two-face worst case of Table VII, pending manufacturer confirmation.

J. Cost and Series Feasibility

The recurring cost specific to this component is the custom three-piece ferrite set. The winding itself carries no per-part cost: it is a section of the host board, and its price is the twelve-layer stack-up, incurred at board level. Assembly reduces to placing the self-locating core pieces, with no clamping hardware or dedicated fixture (Section III-I). The supplier quotes for the N49 set are 1053 € for five machined sets (211 € per set), 5600 € for fifty, still machined (112 € per set), and 8500 € for one thousand sets manufactured as *pressed* parts (8.5 € per set). The pattern is the expected one: machining from blocks amortizes poorly—a tenfold quantity buys only a factor 1.9 on the unit price—whereas the transition to pressed parts at the thousand-set mark cuts the unit cost thirteen-fold, turning the custom shape from a machining bill into a tooling amortization. The custom core is therefore a prototype-cost penalty, not a series one. The point to secure with the supplier at the pressed transition is dimensional: the $\pm 50\,\mu$m ground-face class assumed in Section III-I applies to machined faces, and the gap-critical step being a differential dimension of a single piece (Section III-I) is what is expected to preserve the inductance spread of Table VII on pressed parts.

IV. 3-D Finite-Element Verification

The analytical sizing of Section III relies on two approximations that 3-D FE removes: (i) a one-dimensional, effective-ratio description of the winding AC resistance (12), and (ii) a spatially uniform core flux density (13). Both loss components of the selected design (Table VI) are therefore extracted from a 3-D FE model tailored to the four-phase FSBB waveform. The reference model resolves the three copper layers that form one turn set—under the sizing hypothesis these carry the whole AC current and set the skin, proximity and fringing-field behaviour, the remaining layers being accounted for analytically by a DC resistance division (Section IV-D). A control solve of the complete twelve-layer stack is also performed to test that hypothesis (Section IV-C).

A. Copper Losses from Per-Harmonic Solves

Because the winding AC resistance is a linear, amplitude-independent function of frequency, it is extracted one harmonic at a time. For each current harmonic k (frequency kF_s), a magnetoquasistatic frequency-domain solve is performed and the coil AC resistance $R_{\mathrm{AC}}(kF_s)$ is read directly from the field solution (real part of the coil impedance), which intrinsically captures skin effect, inter-layer proximity, and the single-sided fringing-field compensation. A quasi-DC solve yields R_{DC}. The copper loss is then recomposed in post-processing from the harmonic RMS currents of the optimized waveform:

$$P_{\mathrm{Cu}} = R_{\mathrm{DC}}\, I_{\mathrm{dc}}^2 + \sum_{k\geq 1} R_{\mathrm{AC}}(kF_s)\, I_{k,\mathrm{rms}}^2. \tag{15}$$

This mirrors the analytical split (10) but replaces the effective ratio (12) by the FE-computed, frequency-resolved resistance.

B. Core Losses from a Field-Sensitivity Map

Summing core losses harmonic by harmonic would be invalid (Section III-G). Instead, the linearity of the magnetic problem—the ferrite operates well below saturation—is exploited: a single quasi-DC solve at a reference current I_{ref} yields, for every mesh element e of the core, the field sensitivity

$$\left.\frac{\partial B}{\partial I}\right|_e = \frac{\|\mathbf{B}\|_e}{I_{\mathrm{ref}}} \quad [\mathrm{T/A}]. \tag{16}$$

Since the field distribution scales with the instantaneous current, the local flux-density waveform of each element is reconstructed from the *true* optimized current waveform $i_L(t)$:

$$B_e(t) = \left.\frac{\partial B}{\partial I}\right|_e i_L(t). \tag{17}$$

Each element waveform is evaluated *once* with MagNet-Hub at the fundamental frequency F_s, and the loss is integrated over the mesh:

$$P_{\mathrm{Fe}} = \sum_e p_v\big(B_e, F_s, T\big)\, V_e, \tag{18}$$

where V_e is the element volume. This evaluates the core loss on an arbitrary excitation—rather than on summed sinusoids—from a single field solve; the DC bias is removed prior to

evaluation, consistent with the zero-mean training of the loss model. The figure reported below takes for i_L the fundamental alone, at its peak $\hat{I}_1 = 8.15\,\mathrm{A}$, the harmonics above the first carrying under $5\,\%$ of the AC squared current; evaluating the complete four-phase waveform in (17) is the cross-check. The per-harmonic solves of Section IV-A are thus used *only* for the copper loss. Figs. 9 and 10 show the FE current density in the winding and the flux density in the core.

C. Analytical vs. 3-D FE Comparison

Table VIII compares the analytical (*literal*) winding model with the 3-D FE extraction, both taken on the *final* geometry: the three-piece core as drawn, assembly clearances included. Three observations follow. First, the inductance settles at $0.957\,\mu\mathrm{H}$, $4\,\%$ below target: with the gap set on the complete assembly rather than on the ideal reluctance model, the parasitic clearances are absorbed by construction. Second, the FE DC resistance of one turn set, $9.59\,\mathrm{m\Omega}$ from a quasi-DC solve, is $4\,\%$ below the analytical estimate, whose mean turn length and current-spreading assumptions are slightly conservative. Third, the FE AC resistance at the fundamental is $15.5\,\mathrm{m\Omega}$: an AC-to-DC ratio of 1.62, against the 1.90 carried by the N^2 sizing law (12). The single-sided compensation therefore removes a substantial part of the proximity penalty, but not all of it, and the calibrated ratio is conservative by $15\,\%$ at $N = 3$ rather than by a wide margin—a useful confirmation that the sizing law is neither optimistic nor unusable.

A second solve, resolving the complete twelve-layer stack, tests the current-sharing hypothesis of Section IV-D directly. At the terminals the DC resistance divides exactly by the number of sets ($9.59/4 = 2.40$ against $2.41\,\mathrm{m\Omega}$ extracted), confirming uniform DC sharing. The AC resistance does *not* follow: $12.8\,\mathrm{m\Omega}$ at the terminals against $15.5\,\mathrm{m\Omega}$ for a single set, a reduction of $17\,\%$ where equal sharing would give $75\,\%$. At $450\,\mathrm{kHz}$ the AC current therefore stays almost entirely in the sets nearest the gap, exactly as assumed in (20): the bound the sizing treats as conservative is very nearly the operating point, and the twelve-layer budget of Table IX is validated rather than merely bounded. Recomposed from (15) on the re-optimized waveform, the copper loss is $797\,\mathrm{mW}$ at $60\,^\circ\mathrm{C}$, $22\,\%$ below the analytical $1026\,\mathrm{mW}$ —the margin coming from F_R, 1.62 extracted against 1.90 assumed, and not from any redistribution.

The core-loss map (18), run on the same as-drawn geometry, moves in the opposite direction: $1121\,\mathrm{mW}$ against the $636\,\mathrm{mW}$ of the lumped model (13). The classical expectation—a lumped model made conservative by the dilution of the flux in the yokes—does not hold here, although the dilution itself is real: the volume-averaged flux amplitude comes out at $86\,\mathrm{mT}$ against the $106\,\mathrm{mT}$ centre-leg value of (13) for the fundamental. But the loss density grows faster than B^2, so the integral is dominated by the regions where the flux must cross the assembly clearances, locally up to $0.38\,\mathrm{T}$: evaluated on the field map, this spatial spread alone raises the loss by some $20\,\%$ over the uniform-flux value. The as-drawn ferrite volume, $47\,\%$ above the magnetic-model volume of Table VI, accounts for most of the remainder; the $25\,^\circ\mathrm{C}$ evaluation temperature, pessimistic for a MnZn ferrite whose loss minimum lies near $80\,^\circ\mathrm{C}$, makes the figure conservative. The recomposed total, $1.92\,\mathrm{W}$, holds the $2\,\mathrm{W}$ target, $15\,\%$ above the analytical budget and on a different split between copper and core, which the measurements of Section V will arbitrate.

TABLE VIII
ANALYTICAL (LITERAL) VS. 3-D FE, $N = 3$ FINAL GEOMETRY†

Quantity	Literal	3-D FE	Dev.
L (μH)	1.00^a	0.957	$-4\,\%$
R_{DC}, one set (mΩ)	9.97	9.59	$-4\,\%$
$R_{\mathrm{AC}}(F_s)$, one set (mΩ)	18.94	15.5	$-18\,\%$
$F_R = R_{\mathrm{AC}}(F_s)/R_{\mathrm{DC}}$, one set	1.90	1.62	$-15\,\%$
R_{DC}, terminals (mΩ)	2.49	2.41	$-3\,\%$
$R_{\mathrm{AC}}(F_s)$, terminals (mΩ)	18.94^b	12.8	$-32\,\%$
P_{Cu} (mW, $60\,^\circ\mathrm{C}$)	1026	797	$-22\,\%$
P_{Fe} (mW)	636	1121	$+76\,\%$
P_{tot} (mW)	1662	1918	$+15\,\%$

†Part as drawn, $500\,\mu\mathrm{m}$ gap, assembly clearances included. Resistances at $20\,^\circ\mathrm{C}$: FE R_{DC} from a quasi-DC (1 kHz) solve, FE R_{AC} at $F_s = 450\,\mathrm{kHz}$; the literal $R_{\mathrm{AC}}(F_s)$ applies the calibrated effective ratio (12). ^{a}Sizing target. ^{b}No-sharing bound of (20). Loss rows on the worst-case waveform re-optimized at $0.957\,\mu\mathrm{H}$ ($I_{\mathrm{dc}} = 10.08$, $I_{\mathrm{rms}} = 11.67$ A), copper scaled to $60\,^\circ\mathrm{C}$; FE core loss at $25\,^\circ\mathrm{C}$, MagNet-Hub (N49) on the field-sensitivity map of the as-drawn geometry, excited by the fundamental at $\hat{I}_1 = 8.15\,\mathrm{A}$.

D. Twelve-Layer Stack with Parallel Windings

The board stacks four identical three-layer turn sets—twelve layers, paralleled at the terminals; this is the winding assumed throughout Section III, and this subsection isolates its contribution. At $70\,\mu\mathrm{m}$ copper and $100\,\mu\mathrm{m}$ dielectric the stack fills $2.1\,\mathrm{mm}$ of the $3.3\,\mathrm{mm}$ window (6); the magnetic geometry, the gap and hence P_{Fe} are unchanged.

For the DC current the four windings share equally and the DC resistance is divided by four,

$$R_{\mathrm{DC}}^{(12)} = \frac{R_{\mathrm{DC}}^{(3)}}{n_p} = \frac{11.23}{4} = 2.81\,\mathrm{m\Omega}, \tag{19}$$

with $n_p = 4$ parallel sets. For the AC harmonics the sharing is *not* uniform: at $450\,\mathrm{kHz}$ the copper thickness is comparable to the skin depth and the layers nearest the gap present the lowest impedance, so the AC current concentrates rather than spreading over the twelve layers. We therefore retain the AC loss of the three resolved layers unchanged, which is the conservative bound—any real sharing can only reduce it:

$$P_{\mathrm{Cu}}^{(12)} = \frac{R_{\mathrm{DC}}^{(3)}}{n_p}\, I_{\mathrm{dc}}^2 + F_{R,\mathrm{eff}}\, R_{\mathrm{DC}}^{(3)} \sum_{k\geq 1} I_{k,\mathrm{rms}}^2. \tag{20}$$

The resulting budget is given in Table IX: the DC copper loss falls from 1141 to $285\,\mathrm{mW}$ with the AC term held at $740\,\mathrm{mW}$, i.e. $-45\,\%$ on P_{Cu}. The parallel winding is not an optional refinement: a single three-layer set would dissipate $2.52\,\mathrm{W}$,

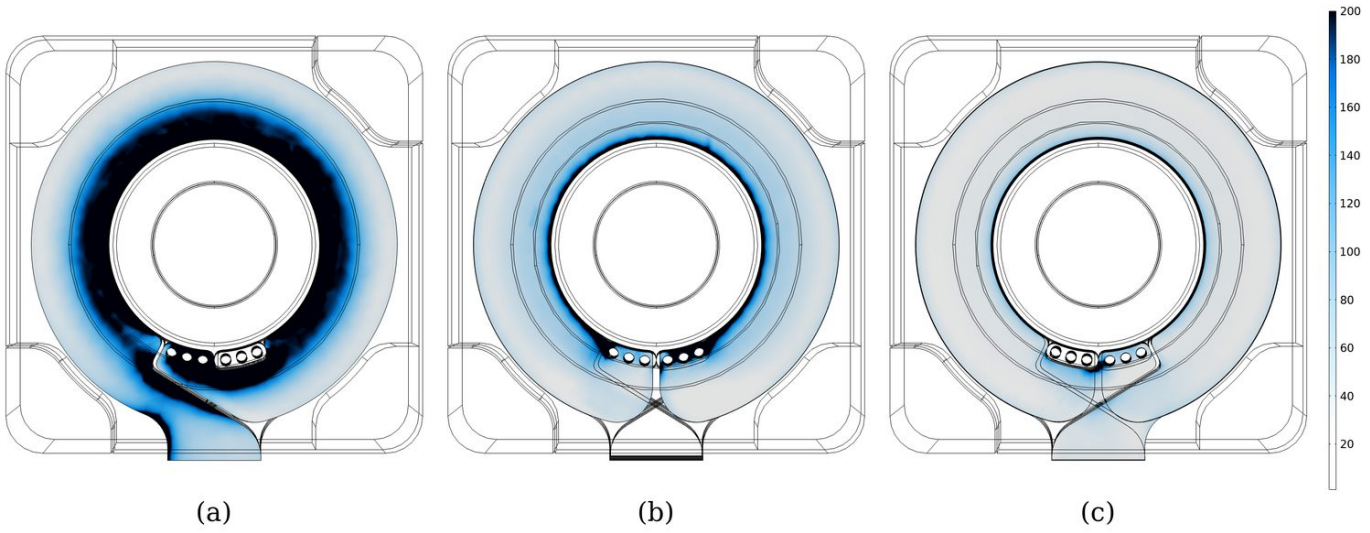

Fig. 9. 3-D FE current-density magnitude $|J|$ in the three copper layers of the resolved turn set, final geometry, at the fundamental frequency ($F_s = 450\,\mathrm{kHz}$) and at the peak of the first harmonic ($\hat{I}_1 = 8.7\,\mathrm{A}$): (a) layer 1, (b) layer 2, (c) layer 3; shared scale in $\mathrm{A/mm^2}$. The single-sided compensation recovers a nearly uniform distribution in the compensated layer, while the remaining layers retain the residual proximity-driven crowding at the track edges discussed in Section III-E.

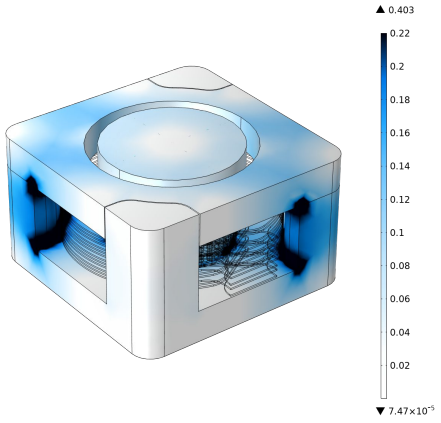

Fig. 10. 3-D FE flux density in the core, three-piece geometry as drawn, assembly clearances included, excited by the worst-case fundamental ($\hat{I}_1 = 8.70\,\mathrm{A}$, Table III). The density is highest where the flux crosses the corner-post clearances and lowest in the outer yokes, in contrast to the uniform-flux assumption of (13). Scale in T, clipped at $0.22\,\mathrm{T}$; the local maximum $0.40\,\mathrm{T}$ occurs at the clearances.

TABLE IX
COPPER LOSS BUDGET: THREE RESOLVED LAYERS VS. TWELVE-LAYER STACK

Quantity	**3 layers**	**12 layers**	**Dev.**
Parallel turn sets n_p	1	4	
Winding height (mm)	0.51	2.14	
R_{DC} (mΩ)	11.23	2.81	$-75\,\%$
$R_{\mathrm{DC}}\, I_{\mathrm{dc}}^2$ (mW)	1141	285	$-75\,\%$
AC term (mW)	740	740	$0\,\%$
P_{Cu} (mW)	1881	1026	$-45\,\%$
R_{AC} eff. (mΩ)	13.80	7.52	$-45\,\%$
P_{Fe} (mW)	636	636	$0\,\%$
P_{tot} (mW)	2517	1662	$-34\,\%$

Worst-case waveform re-optimized at $0.957\,\mu$H, $I_{\mathrm{dc}} = 10.08\,\mathrm{A}$, $I_{\mathrm{rms}} = 11.67\,\mathrm{A}$, ρ_{Cu} at $60\,^{\circ}\mathrm{C}$, $F_{R,\mathrm{eff}} = 1.90$ (sizing value). The AC term is held at its three-layer value, a conservative bound.

$26\,\%$ above the budget, whereas the twelve-layer stack lands at $1.66\,\mathrm{W}$, $17\,\%$ under it—at no size cost, since the extra copper occupies window height the gap placement requires anyway. The complete-stack FE solve of Section IV-C confirms the no-sharing bound to be close to the truth: the terminal AC resistance comes out at $12.8\,\mathrm{m\Omega}$ against the assumed $15.5\,\mathrm{m\Omega}$, so the AC loss is over-estimated by only $17\,\%$ and the budget above stands.

V. EXPERIMENTAL VALIDATION

The prototype inductor is currently in manufacturing. This section will report the winding impedance (R_{AC} versus frequency, inductance versus DC bias and against the tolerance budget of Table VII) and the converter efficiency at the worst-case operating point, confronting the predictions of Sections III and IV with measurement and closing the like-for-like comparison with the litz-wire baseline of Table IV, on the same instrument and method. These results are awaiting delivery of the parts.

The thermal characterization—infrared imaging under worst-case load and hot-spot thermal-resistance extraction—will be presented orally at the conference.

VI. CONCLUSION

This paper has presented a complete design flow for the planar buck-boost inductor of a 200 W FSBB converter rated up to 210 W. A timing optimizer enforcing fixed-dead-time ZVS identifies the worst-case current waveform ($I_{\mathrm{rms}} = 12.14\,\mathrm{A}$ at $V_{\mathrm{in}} = 21\,\mathrm{V}$, $P_{\mathrm{out}} = 210\,\mathrm{W}$), and an analytical design-space

exploration—Dowell-based effective AC resistance, MagNet-Hub core loss on the time-domain $B(t)$, and a core height constructed from the normalized gap placement—selects the footprint-minimal design under the $2\,\mathrm{W}$ budget: a three-turn winding in four parallel sets on a $11.3 \times 11.3 \times 6.5\,\mathrm{mm}$ core ($619\,\mathrm{mm}^3$, $2.9\,\mathrm{g}$, $-73\,\%$ versus the litz-wire baseline) implementing a single-sided fringing-field compensation whose gap placement is fixed by the parametric 2-D FE map. A 3-D FE extraction matched to the FSBB waveform, run on the part as drawn with its assembly clearances, yields $L = 0.957\,\mu\mathrm{H}$—the gap being set on the complete assembly, at $500\,\mu\mathrm{m}$, rather than on the ideal reluctance model—and an AC-to-DC ratio of 1.62 at the fundamental against the 1.90 sizing value. The same extraction resolves the twelve-layer stack and shows the AC current does *not* redistribute over the parallel sets ($12.8\,\mathrm{m}\Omega$ at the terminals against $15.5\,\mathrm{m}\Omega$ for one set), which validates the conservative bound the sizing rests on. The twelve-layer winding, four three-turn sets in parallel, is what holds the $2\,\mathrm{W}$ budget ($2.52 \rightarrow 1.66\,\mathrm{W}$); the recomposed FE budget, $1.92\,\mathrm{W}$, confirms it, a copper loss below the model offsetting a core loss above the lumped prediction. The inductance spreads over $\pm 17\,\%$ (RSS) under standard machining tolerances—the wider gap that absorbs the assembly reluctances buying back a third of the spread—and the identified mitigation is systemic rather than magnetic: a moderate frequency adjustment ($400\,\mathrm{kHz}$) covers the residual at no hardware cost. Electrical and thermal validation against the litz-wire reference is in progress.

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